STATISTICAL ANALYSIS AND OPTIMIZATION IN THE PROCESS/DEVICE/CIRCUIT/SYSTEM MICROELECTRONICS DESIGN

A. Kuleshov[1], V. Nelayev[2], V. Stempitsky[2]
[1]*Belarusian State University*
[2]*Belarusian State University of Informatics and Radioelectronics*
Minsk, Belarus
e-mail: nvv@bsuir.by

Abstract

Methodology and results of statistical analysis and optimization in the joined process/device/circuit/system microelectronics design are presented. A simple example of the cell inverter design illustrates the efficiency of the methodology.

1 Introduction

The current state of microelectronics is characterized by a steady increase in complexity and cost associated with the development of the integrated circuit (IC) design, which in turn leads to a decrease of its "life-time". Therefore, the major problem in microelectronics design today is the need to increase technological sophistication of that which the industry puts out on the market [1, 2].

Optimization of IC's technological parameters essentially means enhancing the manufacturability of its design. The main purpose of this procedure is to provide a high yield level as well as to achieve the best circuit/system performances under specified technology as a result of minimization of their sensitivity to casual deviations of technology parameters. Design for manufacturability is directly connected with getting of as much as possible high yield – the basic economic parameter of IC manufacturing quality. That parameter substantially depends on accuracy and adequacy of computer design of technology, the statistical control of IC manufacturing and the statistical analysis at all stages of process/device/circuit/system (PDCS) design.

Finally, achievement of a high level of IC manufacturability and yield is connected with the solution of two problems of statistical analysis of the design results, and computer and natural experiments. The first, direct problem, is investigation of influence of statistical fluctuations of technological parameters on output performances of PDCS. The aim of second, reverse problem is definition of tolerance of possible deviations of technological parameters provided fluctuations of output PDCS performances in the specified range [2].

However direct statistical modeling of process demands significant computer resources. The idea is in finding an effective mean for construction of approximated dependences of numerical process simulation results (or results of natural experiments) which would allow describing with enough precision results of computer/natural experiments in the form of polynomial series and then can be used at the statistical analysis in the Monte-Carlo loop and optimization at each stage of end-to-end design of PDCS.

The most effective method for solution of that statistical problem is the responses surface methodology – RSM [1].

In this paper the problem is solved for joining of the own methodology for realization of RSM approach with the mentioned standard software for statistical analysis and optimization in the end-to-end design.

The same problem was discussed in the series of investigations [3, 4, 5].

2 Statistical analysis in the end-to-end design

The flow diagram of the joined approach for statistical end-to-end design methodology from process stage to system one is presented at Fig.1. Output performances of each previous stage are used as input parameters for the subsequent design stage.

The input information for a process design stage is technology parameters (P_i) of the separate process operations. These parameters are, for example, doses of impurity implantation, temperature of oxidation process and other parameters of the process flow. Profiles of impurity distributions, geometric parameters including depth of p-n junctions are results of technology design stage executed for manufacturing of specified device. We used SSuprem4, a program package for 2D simulation which is a part of ATHENA module of the Silvaco package.

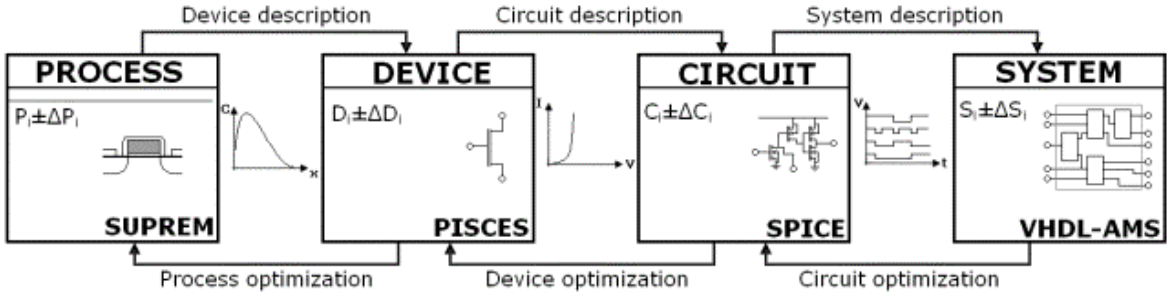

Figure 1: Flow diagram of end-to-end statistical design realization

Simulation of device performances is carried out on the base of process simulation results and is realized by means program PISCES, is the basis for ATLAS module of Silvaco package. Parameters for that stage of end-to-end design are performances of the device model (D_i), such as SPICE-parameters of the MOS-transistor model which values are defined by output parameters of process simulation. Extraction of SPICE-parameters is realized with use of own methodology [6].

The next step in the end-to-end design, circuit simulation, is realized by using SPICE program which is the core of modern software complexes, such as Cadence, Mentor Graphics, etc. Influence of fluctuations of the input parameters at circuit simulation stage C_i (SPICE-parameters of the device), which range of deviations was defined at previous design stage, is investigated during statistical analysis in Monte-Carlo loop or in Worst-Case analysis.

The final stage of the end-to-end design is investigation of system output performances. Parameters of this stage are system performances. Specification of parameters

Table 1: Results of output parameters statistical analysis of MOS-transistor structure process simulation obtained by using of RSM polynomial approximation

Parameter	Nominal values	Minimum values		Maximum values	
		Absolute value	Relative tolerance, %	Absolute value	Relative tolerance, %
X_j, μm	0.1730	0.1726	0.7	0.1821	5.3
V_{TH0}, V	0.5080	0.4714	7.2	0.5537	9.0

for system simulation/design, including initial data for carrying out of the statistical analysis, is performed by use of hardware description language, such as Verilog-AMS.

3 Example of end-to-end statistical design

Described methodology of end-to-end PDCS statistical design was tested on a simple invertor cell formed on basis of MOS-transistor. Simulation of MOS-transistor technology and approximation of results by second power polynomial in RSM approximation were executed. Three significant technological parameters which define output performances of MOS-transistor technology (depth of p-n-junction X_j at the source/drain region and threshold voltage V_{TH0}) have been chosen, as input factors P_i (see Fig. 1): dose of channel doping implantation, D_{CH};dose of source/drain doping implantation, D_{DS};temperature of annealing for diffusion redistribution of impurity implanted in channel, T. Here X_j and V_{TH0} are also SPICE-parameters of the investigated MOS-transistor. As a result of RSM analysis, polynomial approximated dependences X_j and V_{TH0} vs. D_{CH}, D_{DS} and T were obtained.

Presented in Table 1 results show the displacement of "central" values of output performances X_j and V_{TH0} as a result of statistical analysis of input parameters fluctuations influence D_{CH}, D_{DS} and T in comparison with "central" values specified at the initial design of experiments.

Thus, under statistical analysis at a following stage, a device design stage, the central value of SPICE-parameter X_j should be equaled to $(0.173 + 0.182)/2$ μm $=$ 0.176 μm, and tolerance value is equaled to $\pm(0.7 + 5.3)/2\% = \pm 3\%$. Note, that the central value and the deviation of parameter X_j deduced for polynomial approximation from results of computer experiments according to the design of computer experiments were 0.173 μm and $\pm 5\%$ respectively. Corresponding calculations for SPICE-parameter V_{TH0} give $(0.471 + 0.554)/2$ V $= 0.512$ V $\pm 8.1\%$ against 0.508 V $\pm 5\%$.

The first step of the statistical analysis for device (here n-MOS transistor) is to "transform" process parameters in I-V transistor performances by use of ATLAS module of Silvaco package. The second step is to extract SPICE-parameters of investigated n-MOS transistor from obtained I-V performances by subsequent procedure of optimization [6] or by use procedure for the analytical processing of I-V performances incorporated in module ATLAS (V_{TH0} parameter). Procedure and results obtained in

result of extraction of SPICE-parameters X_j taking into account tolerances of V_{TH0} and N_{SUB} were described in previous step.

Simulation of inverter circuit formed on the basis of n-MOS-transistor was carried out by means of Cadence package. Investigation of statistical tolerance of the output performances (the time diagram) of the inverter is realized as a statistical analysis in the Monte-Carlo loop (MC-analysis). The tolerance of the inverter output voltage with taking into account deviations of investigated SPICE-parameters is $\pm 2.5\%$.

4 Conclusion

The statistical analysis methodology in the end-to-end design of process/device/circuit/system was presented. It is shown, that the described and tested methodology and the developed software allow with sufficient accuracy and reasonable computer resources to carry out the analysis of performance tolerances at all design stages on the base of information about fluctuations of process parameters.

The proposed solution of reverse, optimization problem, allows defining restrictions imposed on process parameters, depending on specifications of system performances. Obtained results can be used for statistical design for manufacturability in conditions of real and "virtual" manufacturing of microelectronics products.

References

[1] Kouleshoff A., Malyshev V., Nelayev V., Stempitsky V. Statistical design and optimization of IC technology. *Microelectronics* (Russian J.). 2003, Vol. 32, No 1. P. 47-61.

[2] M. Krasikov, V. Nelayev, Stempitsky V., V. Syakerckii, End-to-end statistical process/device/circuit/system design. *Proc. of SPIE*. 2009, Vol. 7377-40.

[3] Kuzmicz W., Piwowarska E., Pfitzner A., Kasprowicz D. Leakage currents and static power consumption in nanometer CMOS ICs. Proc. of IEEE East-West Design and Test Symposium, EWDTS'07, 7-11.09.2007, Yerevan, Armenia. P. 152-157.

[4] Fujita T., Onodera H. A method for linking process-level variability to system performances. *IEEE Trans. Fundamentals*. 2000, Vol. E-83a, No. 12. P. 2592-2599.

[5] Koskinen T., and Cheung P.Y. Hierarchical tolerance analysis using statistical behavioral models. *IEEE Trans. Computer-Aided Design of Integrated Circuits and systems*. 1996, Vol. 15, No. 5. P. 506-516.

[6] Krasikov M., Malyshev V., Nelayev V. Parameter verification of physical-mathematics models in microelectronics design tools. Proc. of Int. Conf. "Computer Aided Design of Discrete Devices", November 14-15, 2007, Minsk, Belarus. Vol. 1. P. 223-227.