AN APPROACH TO REDUCE THE POWER CONSUMPTION DURING SIGNATURE ANALYSIS

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Abstract. Power consumption of digital systems may increase significantly during testing. In this paper power consumption of the LFSR-based signature analysis register for scan-based BIST schemes is analysed. To reduce the power consumption of BIST scheme an alternative signature analyser is proposed. This solution can be easily integrated into an existing design flow and does not have any negative impact on test speed and system speed.

1. Introduction

In recent years, power consumption gained popularity as one of the major concerns of VLSI designers. The primary driving factor for this trend has been the diffusion of battery-powered portable devices such as laptop computers, audio and video-based multimedia products and cellular phones. For this new class of battery-powered portable devices, average power consumption is a critical design concern, since it determines the battery life. A strong pressure for reducing power dissipation is also coming from producers of high-end systems. The cost associated with packaging and cooling of such devices is huge: since core power consumption must be dissipated through the package, increasingly expensive cooling and packaging is required. Unless power consumption is reduced, the resulting heat will limit the systems performance [9].

Researches report that the switching activity of the circuit during self-test is significantly increased compared to normal operation, and therefore leads to increased power consumption which often exceeds specified limits [6]. The problem of energy or power consumption minimization during BIST has already been addressed in several publications. In [11], the author presents a test scheduling approach that takes into consideration the power consumption. To reduce power during scan mode the new scan path architecture has been proposed in [8]. There are a set of solutions to eliminate useless pseudo random patterns during the test mode [6, 5] to keep the same fault coverage at acceptable test length and as the result at lower level of power consumption. Intensive research efforts have been devoted to develop techniques and algorithms to reduce average power consumption at different levels of abstraction [1,2]. The proposed approaches target the average power consumption during normal circuit operations only, but they do not concern power consumption during test.

Built-In Self Test (BIST) schemes contain signature analyser (SA). SA is usually based on the linear feedback shift register (LFSR). This is due to the fact that an LFSR can be built with little area overhead. There is another advantage – LFSR is also used as test pattern generator (TPG) to apply pseudo-random test stimuli to the circuit under test (CUT).

The most commonly used self-test technique is "test-per-scan" technique (*Fig. 1*). A TPG generates a bit sequence, which is feed into the scan path. The contents of the scan path after shift-in procedure serves as a test pattern for the CUT. The responses of the CUT are captured by the scan path in parallel, and serially fed into a signature analysis register

(SA). The first l>0 stages of scan path for most cases are used as an inputs for the CUT and the rest are operating in a both mode for the test generation (inputs) and response evaluation (outputs) of CUT. Entire length of the scan path is s>l.

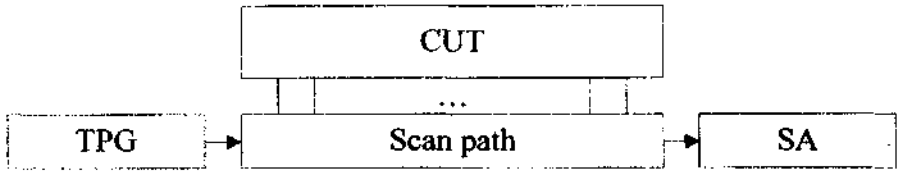

Fig.1: Scan-Type BIST architecture.

Scan based BIST architectures are popular because of their low impact on area and performance. However, scan based architectures are expensive in power consumption as each output response analysis requires a large number of shift operations with a high circuit activity.

In this paper we propose an approach to reduce the amount of power consumed by the signature analyzer. The key idea is to use a signature analysis register with variable number of inputs (VISAR – variable inputs signature analysis register)[10]. The main property of the VISAR is the fact that number of memory cells is determined by the generating polynomial degree only and it does not depend on the number of inputs. This approach allows reducing the power consumption without influence on the signature accuracy. Moreover it has no impact on the test speed as well as on the system speed.

The paper is organized as follows. In section 2, the power consumption issue and weighted switching activity modeling are investigated and the key idea behind the proposed solution is described. The power reduction estimation is in section 3. Finally section 4 draws some conclusions.

2. Power consumption and WSA modelling

Power dissipation in CMOS circuits can be classified into static and dynamic. As have been shown before [3], dynamic power is the dominant source of power consumption, what is due to short circuit current and charging and discharging of load capacitance during output switching.

The power consumed at node j per switching is $1/2C_jV^2_{dd}$ where C_j is the equivalent output capacitance and V_{dd} is the power supply voltage [4]. Hence, a good estimation of the energy consumed during f_j switchings at node j is $1/2f_jC_jV^2_{dd}$. Nodes connected to more than one gate are nodes with higher parasitic capacitance C_j is assumed to be proportional to the fan-out of the node s_j [6]. The resulting expression for consumed energy E_j at node j is:

$$E_j = 0.5s_jf_jC_0V^2_{dd}, \quad (1)$$

where C_0 is the minimal output load capacitance for the case when s_j=1.

According to the last expression, the estimation of the energy consumption at the logical level requires the calculation of the fan-out s_j and the number of switching f_j on the node j.

The product s_jf_j is named Weighted Switching Activity (WSA) of node j and is used as a metric for the power consumption at the node, due to it is the only variable part in the expression (1). Thus the WSA generated in the circuit after application of one clock pulse can be expressed by the equation:

$$WSA_{cl} = \sum_{j=1}^{n} s_j f_j \qquad (2)$$

Let us consider now the case of signature analysis by the Linear Feedback Shift Register (LFSR). The metric WSA per one clock $f_{cl}=1$ (WSA_{cl}) for LFSR can be used as the metric WSA per one bit of the CUT output response (WSA_B) and it can be estimated taking into account that there are two types of LFSR nodes: control nodes for clock pulses which are with the highest switching activities $f_p=2f_{cl}$ due to the clock pulse has two switchings at both pulse edges, at rising and falling. Logical nodes have the switching activity $f_i=0.5f_{cl}$, where i is the number of logical node. Here we took into account that the probability of switching at LFSRs logical node equals to *0.5*. [7]. For example, let us consider SA on the LFSR for the generating polynomial $\varphi(x)=1+x+x^3$ (see *Fig. 2)*.

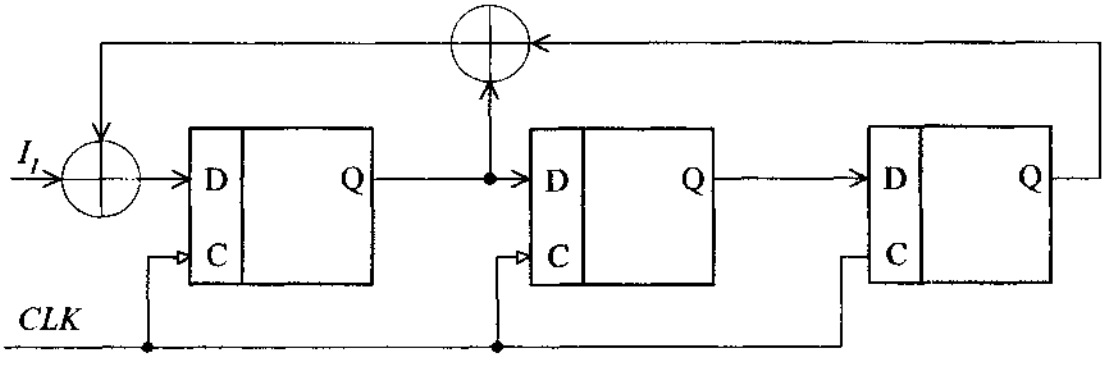

Fig.2: LFSR-based signature analyzer.

For the general case all nodes of LFSR can be presented as four subsets. The first subset is the control inputs with the m nodes *(S1=m, m*-the degree of the generating polynomial*)*, the second subset consists of m LFSR`s flip-flops data inputs *(S2=m)*, the next subset includes inputs of the feedback circuit constructed on the exclusive or gates, and the last subset consists of one input node I_1 *(S4=1)*. For the above presented example *S1=3, S2=3, S3=3,* and *S4=1*. Taking into account the last conclusions concerning the LFSR`s nodes and their switching activities WSA per one bit (WSA_B), namely the WSA generated in the LFSR while compression of one new bit of the CUT output response, can be rewritten as:

$$WSA_R = 2f_{cl}S1+0.5f_{cl}(S2+S3+S4)=2f_{cl}m+0.5f_{cl}(m+S3+1)=[f_{cl}=1]= \\ =0.5(5m+S3+1). \qquad (3)$$

For the above presented example (*Fig.2*) WSA_B is calculated as $WSA_B=9.5$.

Taking into account the last expressions we can propose some approaches to reduce the power consumption through the reduction of f_{cl} – the number of clock pulses per one input bit being analyzed, what is according to our understanding practically the only constructive way to design low power consumption LFSR-based test pattern generators. The key idea behind this proposal is based on using of the VISAR which requires only one clock pulse to perform the same transformations of the input sequence as the LFSR performs during $l>1$ clocks.

Let us construct signature analyzer that compresses three bits per clock and generates the same signature as the LFSR-based one. According to the methods [10] the analyzer must be based on the same polynomial $\varphi(x)=1+x+x^3$. The SA for this case is shown in *Fig.3*.

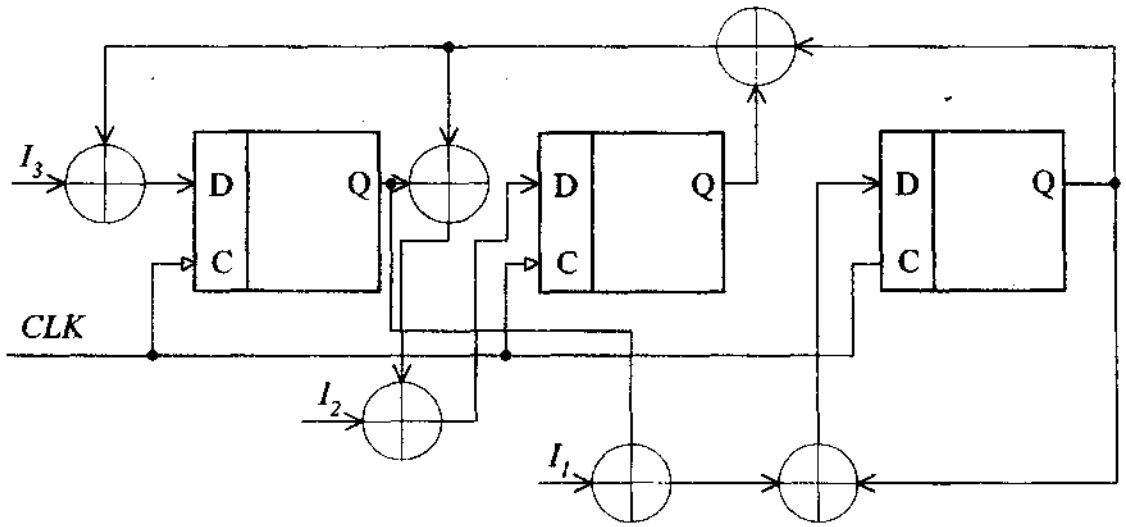

Fig.3: Three bits per clock VISAR-based analyzer.

Comparing hardware overhead in scan based BIST with the LFSR-based signature analyzer TPG (*Fig.2*) and the last one (*Fig.3*) we can see that with proposed analyzer there is no need in shift-out procedure, because next part of sequence can be captured directly the CUT. The requred number of bits $d>1$ to be analyzed per clock can be easily changed without affecting the number of the analyzer's triggers. A WSA_B for the last structure can be calculated as:

$$WSA'_B = (2f_{cl}S1+0.5f_{cl}(S2+S3'+S4))/d=[S4=d, f_{cl}=1]=(5m+ S3')/2d+0.5. \quad (4)$$

For the above presented example (*Fig.3*) is calculated as $WSA'_B=6.5$. Thus, using this signature analyzer instead of LFSR power savings in $Q=9.5/4.83=1.97$ times can be achieved. Let us consider the experimental results now.

3. Experimental results

The results of WSA_B estimation for the cases of the generating polynomials $\varphi(x)=1\oplus x\oplus x^4$(the lower graph), $\varphi(x)=1\oplus x^3\oplus x^5\oplus x^8$ (the middle graph) and $\varphi(x)=1\oplus x^2\oplus x^7\oplus x^8\oplus x^{12}$(the upper one) are shown in *Fig.4*.

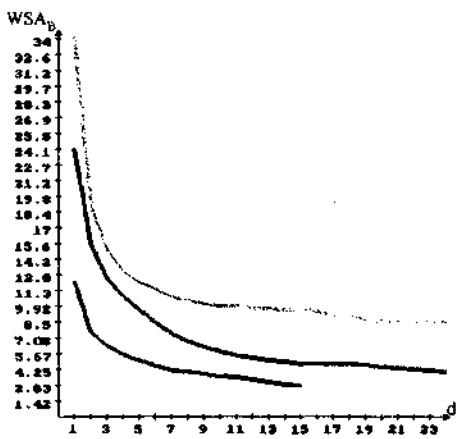

Fig. 4: Dependence of WSA_B on the number of bits compressed per clock.

The points with $d=1$ horizontal coordinate show the values of WSA_B for the cases

of using standard LFSR that compresses only one bit per clock. The effectiveness of using the proposed approach is confirmed by a quantity of experiments, carried out during the research work.

4. Conclusion

The theoretical analysis and experimental results show that using the VISAR instead of LFSR is a very effective solution to design low-power BIST scheme. Classic scan based BIST architectures are expensive in power consumption as response requires a large number of shift-out operations with a high circuit activity. Using VISAR does not require these shift-out procedures because each response is received by the analyzer in parallel.

This approach can be easily integrated into an existing design flow, and does not affect the efficiency of the BIST architecture, since it saves power without reducing the fault coverage.

References

[1] M. Aladina, J. Monteiro, S. Devadas, A. Ghosh, M. Papaefthymiou, "Precomputation-based sequential logic optimization for low power", *ACM/IEEE International Workshop on Low Power Design*, (1994), 57-62.

[2] L. Benini, G. De Micheli, "Transformation and synthesis of FSMs for low power gated clock implementation", *ACM/IEEE International Symposium on Low Power Design*,(1995), 21-26.

[3] A.K.Chandrakasan, S.Cheng, R.W.Brodersen, "Low-Power CMOS Digital Design", *IEEE Journal of Solid-State Circuits*, 27, 4, 473-484.

[4] M.A.Cirit, "Estimating Dynamic Power Consumption of CMOS Circuits", *ACM/IEEE International Conference on CAD*, (1987),534-537.

[5] S.Gestendurfer, H.-J.Wunderlich, "An Approach to Reduce the Power Consumption During Scan-Based BIST", *IEEE European Test Workshop*,(1999).

[6] P.Girard, L.Guiller, C.Landrault, S.Pravossoudovitch, "A Test Vector Inhibiting Technique for Low Energy BIST Design", *Proceedings of IEEE VLSI Test Symposium*, (1999), 407-412.

[7] S.W.Golomb, *Shift Register Sequences*. Holden Day, (1967).

[8] A.Hertwig, H.J.Wunderlish, "Low Power Serial Built-In Self-Test", *IEEE European Test Workshop*,(1998), 49-53.

[9] M.Pedram, "Power Minimization in IC Design: Principles and Applications", *ACM Transaction on Design Automation of Electronic Systems*, 1, 1, (1996), 3-56.

[10] V.N. Yarmolik, "Testing and diagnostics of computer's digital circuits". Minsk: Nauka i Technika, (1988), 215-221.

[11] Y. Zorian, "A Distributed BIST Control Scheme for Complex VLSI Devices", *Proceedings of IEEE VLSI Test Symposium*,(1993), 4-9.