A SWITCHING ACTIVITY REDUCING TECNIQUE FOR THE SIGNATURE ANALYZER

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Abstract. This paper presents new solutions for reducing the power consumption of built-in self-test (BIST) environment such as signature analyzer (*SA*). The key idea behind this technique is based on the designing a new *SA* structure for compressing several test responses bits per one clock pulse. The proposed method can be used within *"test-per-clock" BIST* architecture, as well as may be extended for the *"test-per-scan" BIST* technique.

Introduction

In recent years, for modern *VLSI* circuits, due to a wide range of critical applications, the design task no longer concentrate over area/performance trade-off only. There are new variables becoming of primary concerns, and power consumption is more important now for critical applications, such as mobile computing devices and cellular phones.

Several approaches of low power *BIST* have been proposed. In [1], the author presents a test scheduling approach that takes into consideration the power consumption. For general *BIST* structure a new test pattern generator is proposed [2] to reduce the circuit inputs activity without affecting test efficiency, thus reducing power consumption.

There is a set of solutions to eliminate useless pseudo random patterns during the test mode [3, 4, 5] to keep the same fault coverage at acceptable test length as the result of the lower level of power consumption.

The most spread and the best known are *scan designs* techniques. They assume that during testing mode all memory elements (flip-flops and latches) in a sequential circuits are connected into one or more shift registers or scan paths. By far *LFSR* is the most popular device for generation pseudo-random test sequences. Also a structure of *LFSR* can be modified to accept an internal input in order to work as a polynomial divider (called Signature Analyzer - *SA*). That is why the sufficient amount of energy is consumed during the shifting mode, for the bit stream generation, output response compaction and bit stream shifting into the scan. In [6] was shown that *BIST* hardware may consume up to 70 % of total energy during testing mode.

This paper presents new solutions for reducing the switching activity of *BIST* environment for the scan-organized *BIST* architectures such as Signature Analyzer.

Switching energy estimation

Power dissipation in *CMOS* circuits can be classified into static and dynamic. As have been shown before [7], dynamic power is the dominant source of power consumption, what is due to short circuit current charging and discharging of load capacitance during output switching. The power consumed at node j per switching is:

$$E_j = 1/2 C_j V_{dd}^2 \quad (1)$$

where C_j is the equivalent of output capacitance and V_{dd} is the power supply voltage [8]. Nodes connected to more than one gate are nodes with higher load capacitance. C_j can be calculated as:

$$C_j = s_j C_0 \quad (2)$$

where C_0 is the standard load capacitance for the one logical input, s_j is fan-out node j. The resulting expression for consumed energy E_j at node j is:

$$E_j=1/2 s_j f_j C_0 V^2_{dd} \quad (3)$$

where f_j is the number of switching on the node j. The product $s_j f_j$ named Switching Activity *(SA)* of node j is used as a metric of the power consumption at the node j, due to it is the only variable in the energy consumption expression (3).

$$SA_j= s_j f_j \quad (4)$$

The constant component of expression (3) is power of one switching and may be written as

$$E(1)=1/2 C_0 V^2_{dd} \quad (5)$$

The common number of switchings (SA) of the CMOS circuit may be found as the sum of switchings on all its nodes

$$SA= \sum_j SA_j \quad (6)$$

Thus the power consumed of CMOS circuit is

$$E= E(1)\, SA \quad (7)$$

We shall use SA as an estimation of power consumption. For comparison of efficiency of offered techniques we shall use weighted switching activity (WSA). WSA is number of switchings for compressing of one test responses bit.

Scan-based architecture

Let us consider the typical "test-per-clock" scan-based BIST *(Fig.1)*. There are two main components of this architecture [9]: *1)* Test Pattern Generator *(TPG)*, *2)* a compactor. A test pattern generator consists of $m1$-bit *LFSR*, which task is to feed a single $k1$-bit into scan path *SP1 (Fig.1)*. A compactor consists of a $k2$-bit scan path *SP2* which is fed into a signature analyzer with characteristic polynomial of degree $m2$. For all units of this architecture there is one clock source f_{CLK}.

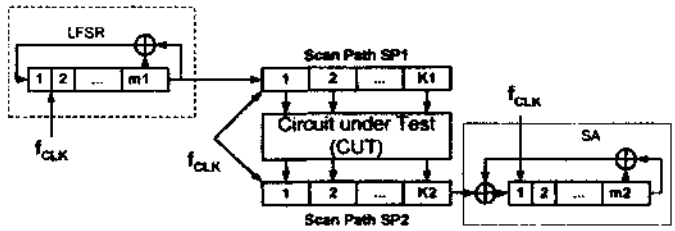

Fig. 1 The typical scan-based architecture

This paper presents a new solution for scan-based *BIST* that allows reducing switching activity of test response compactor which consist of *SP2* and *SA* (fig.1). The key idea behind this approach is based on the designing a new compactor structure for compressing several test responses per one clock pulse.

Switching activity estimation for LFSR-based signature analyzer

Let us now consider the base structure of test response compactor. Usually the compactor consists of scan path with *XOR* gates added to flip-flops, which is fed into the single input *LFSR* or signature analyzer. The example of a 4-bit scan path, which is fed into a 4-bit single input *LFSR* with the characteristic polynomial $\varphi(x)=X^4 \oplus X^3 \oplus 1$ is shown in *Fig.2*.

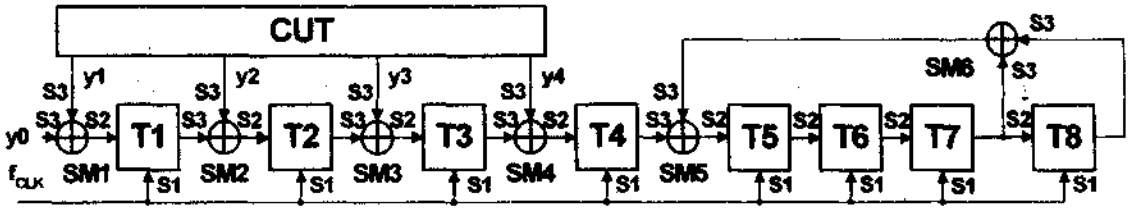

Fig. 2 The base structure of test response compactor

Let us analyse the switching activity of a base structure of test response compactor. We assume that the number of clock pulses is equal to 16. As the *CUT* has four outputs *y1-y4*, 64-bit test response was fed into scan path. We assume that each output of CUT has a probability of 0.5 of being either a 0 or a1. Therefore on each output of the circuit occurs eight switching.

All nodes of this circuit can be presented as 3 subsets. First subset ***S1*** is the clock inputs of the flip-flops *(|S1|=8)*. Second subset ***S2*** consists of data flip-flops inputs *(|S2|=8)*. The next subset ***S3*** includes inputs of the *XOR* gates *(|S3|=12)*. Let's designate switching activity of clock inputs, as SA_{S1}.The number of clock inputs equals 8. The number of clock pulses is equal 16 (each clock pulse twice changes a logical level). Thus, $SA_{S1}=8*16*2=256$. The number of data inputs is equal 8. Thus, $SA_{S2}=8*8=64$. Subset ***S3*** consists of twelve inputs of ***SM1- SM6***, that is $SA_{S3}=12*8=96$. As a results we receive $SA_{SP\_SA}=SA_{S1}+SA_{S2}+SA_{S3}=416$. There are *4*16=64* bit test response was fed into scan path. For the example presented above *(Fig.2)* Weighted Switching Activity (number of switching for compressing one bit test response sequence) can be rewritten as $WSA_{SP\_SA}=416/64=6,5$.

A brief examination of the WSA_{SP_SA} allows to make the conclusion that the most significant part of power consumption is the switchings on inputs of synchronization. Because we can propose some approaches to reduce the power consumption through the reduction of the number of clock pulses for compressing one bit test response sequence. The new structure of test response compactor is described in the following section.

Switching activity estimation for new structure of signature analyzer

Let us analyses the switching activity of the new structure of *SA* (Let's name given structure ***SA2x***). We assume that the number of clock pulses is equal to 16. There is 64 bit of test response were fed into scan path for circuit on fig.2. In the second one (fig.3), 128-bit test responses were fed into scan path.

Switching activity of subsets *S1* has not changed, since $SA_{S1}=8*16*2=256$. The number of inputs of subset *S2* has not changed, but additional switching has occurred on *D*-inputs of flip-flops *T1-T5*. Thus, $SA_{S2}=8*8+5*8=104$. Subset *S3* consists of low switching inputs of *SM1-SM11 (|S3|=11)*, hence $SA_{S3}=11*8=88$. The remaining inputs of *SM1-SM11* have high switching activity. They include subset *S5 (|S5|=11)*, $SA_{S5}=11*16=176$. Subset *S4* consists of four inputs to delay gates *E1-E4*, hence $SA_{S4}=4*16=64$. As a result, $WSA_{SA2x}=688/128=5,375$. Thus the new structure of *SA (SA2x)* has *1.2* times less switching than the basic structure.

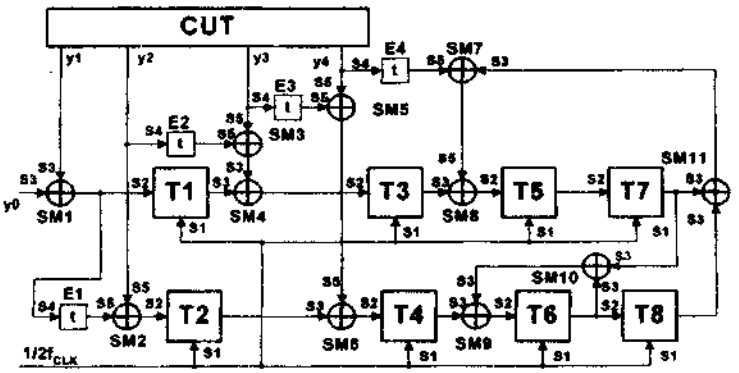

Fig. 3 The new structure of test response compactor (SA2x)

Switching activity reduction estimation

Let us find weighted switching activity for presented above structures for general case. We assume that m is higher degree of characteristic polynomial and s is number of output of CUT. In the first case (fig.2) 64-bit test response were fed into scan path. In the second one (fig.3) 128-bit test response were fed into scan path. The Expression for WSA_{SP_SA} is

$$WSA_{SP\_SA} = (2.5m+3.5s+2)/s \tag{8}$$

Similarly

$$WSA_{SA2x} = (1.25m+2.625s+1.25)/s \tag{9}$$

For the analysis of these expressions we shall enter the following function $w(m,s)$

$$w(m,s) = WSA_{SP\_SA} / WSA_{SA2x} \tag{10}$$

The factor of decreasing of the power consumption for fixed values of s (s=20) and different values of m (m=5..50) are shown in Fig.4. The factor of decreasing of the power consumption for fixed values of m (m=30) and different values of s (s=5..50) are shown in Fig.5.

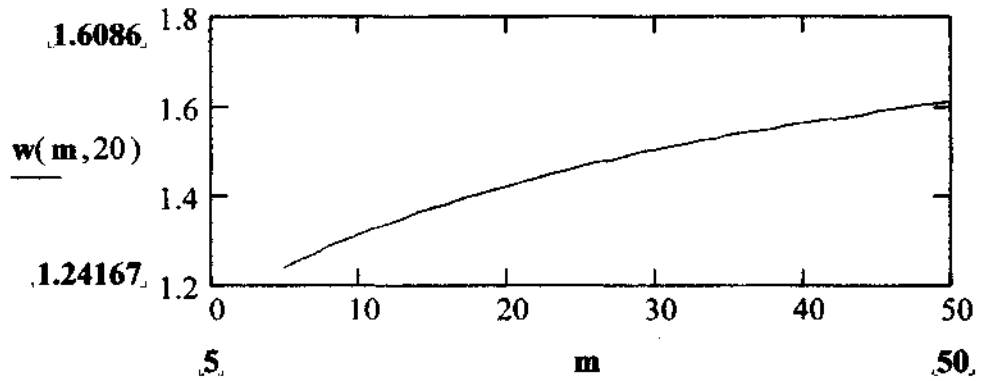

Fig. 4 The factor of decreasing the power consumption for different value of m

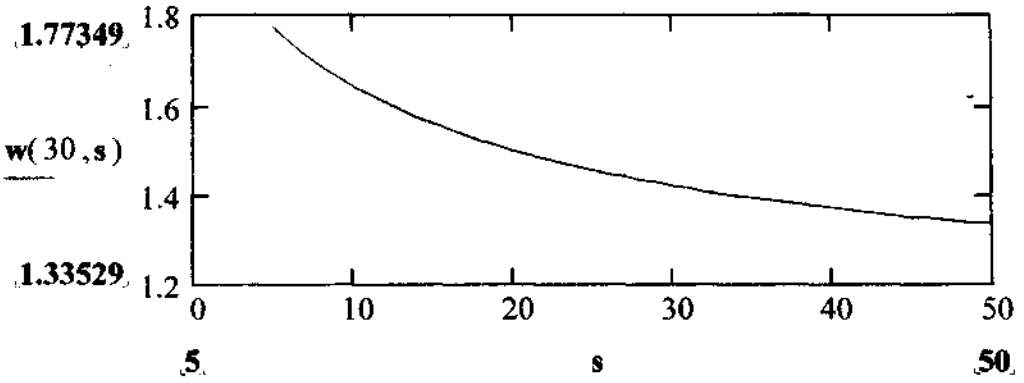

Fig. 5 The factor of decreasing the power consumption for different value of s

Conclusion

In this paper the new architecture of test response compactor hardware for low power design is given.

References

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