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Original article

Simulation of a quasi-ballistic quantum-barrier field-effect transistor based on GaAs quantum wire

Dmitry V. Pozdnyakov[1,a], Andrei V. Borzdov[1,b], Vladimir M. Borzdov[1,c]

[1]Belarusian State University, Minsk, Belarus

[a]pozdnyakovdv@bsu.by, [b]borzdovav@bsu.by, [c]borzdov@bsu.by

Corresponding author: D. V. Pozdnyakov, pozdnyakovdv@bsu.by

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ABSTRACT A new constructive solution of field-effect transistor (FET) with a Schottky barrier in a conducting channel has been identified. The FET is a quasi-ballistic quantum-barrier transistor based on a cylindrical undoped GaAs quantum wire in Al_2O_3 matrix surrounded by a cylindrical metallic gate. A technique for determining the optimal variation of the semiconductor quantum wire diameter along its axis has been developed. The optimal dependence of the nanowire diameter on the spatial coordinate along its axis has been determined providing the possibility of both the elimination of quantum barrier for electrons by the positive gate voltage and the minimization of transistor channel electrical resistance in contrast to a typical FET with a Schottky barrier in its conducting channel. The current-voltage characteristics of the transistor based on GaAs quantum wire with an optimal cross-section have been calculated within the framework of a developed combined physico-mathematical model describing the electron transport in the transistor channel. This model takes into account the nonparabolicity of the semiconductor band structure, the quantum-dimensional effects, and such secondary quantum effects as the collisional broadening and displacement of electron energy levels.

KEYWORDS field-effect transistor, semiconductor quantum wire, quasi-ballistic electron transport.

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1. Introduction

The basic element of digital integrated electronics, which performs the role of a normally open switch, is still a silicon metal-insulator-semiconductor field-effect transistor (MIS FET) with an induced channel [1]. Fulfillment of three basic requirements for such kind of switching elements for further increasing the degree of integration of the micro- and nanoelectronics component base, in particular, reducing geometric dimensions, increasing switching speed, and reducing dissipated power, forces the developers of this kind of device structures to reduce the values of operating voltages on the gate and drain of the transistor [2,3], to select alternative materials for its conductive channel [4–9], to use other principles for controlling its switching [10, 11], and also to search new design and topological solutions [3–19]. At least most of the above requirements can be satisfied by a ballistic nanotransistor with a cylindrical gate, which has the following features [3, 8, 16–20]: 1) the cylindrical conducting channel contains a one-dimensional electron gas under the electric quantum limit conditions; 2) the conductive channel is formed of a very high-tech material with a very high electron mobility; 3) the material of the insulating matrix of the transistor is technologically compatible with the materials of its conductive channel and electrodes; 4) as in a tunnel FET, the height and width of the potential barrier for charge carriers is directly controlled by the gate voltage; 5) in the open state of the transistor its electrical conductivity achieves the maximum possible quantum-mechanical value $g\pi^{-1}\hbar^{-1}e^2$ [21], where g is the degree of electron gas degeneracy, $\hbar$ is the reduced Planck constant, e is the absolute value of the electron charge.

In due time in scientific papers [22, 23] and monograph [24], a design and topological solution satisfying the above mentioned conditions was proposed in the form of a normally open transistor switch based on $Al_XGa_{1-X}As$ with a variable fraction of aluminum in the semiconductor lengthwise the conductive channel of the transistor with optimal geometry. As it was shown in [23, 24], the proposed solution practically achieves the maximum possible theoretical values for such key parameters of the transistor as the subthreshold swing, the channel conductivity and the ratio of electric currents in the open and closed states. The geometry of the transistor considered in [22–24] meets the current production capabilities in the electronics industry. At the same time the necessity of smooth variation of the stoichiometry of $Al_XGa_{1-X}As$ lengthwise the transistor conductive channel, taking into account the possibilities of both molecular beam epitaxy and other methods of forming semiconductor structures with specified physical and chemical properties, limits the range of possible structural and topological solutions for such device structures. In particular, this is why the vertical transistor was considered in [22–24]. But it is possible to control the electron potential energy profile in the conductive channel

of a quantum-barrier transistor not only by changing the stoichiometry of the ternary semiconductor quantum wire, but also by varying its diameter along the wire axis, which determines the local position of the electron subband levels in the semiconductor relative to the bottom of its conduction band [22–24]. And such a method of profiling the effective potential energy of electrons in the conductive channels of quantum-barrier transistors, firstly, removes the limitation on the production of the transistors only in the vertical design and, secondly, expands the range of semiconductors that could be used as base materials for the conducting channels of such kind of device structures.

Thus, in view of the above, the purpose of this work is to optimize a number of topological parameters of a quasi-ballistic FET with a cylindrical metallic gate and one-dimensional electron gas in the conducting channel based on a cylindrical undoped GaAs quantum wire with a variable cross-section lengthwise the conductive channel of the transistor, as well as to calculate its current-voltage characteristics (CVC).

2. Theory

As a starting point, let's consider the design of a vertical ballistic quantum-barrier FET proposed in refs. [22–24]. Its schematic view is shown in Fig. 1.

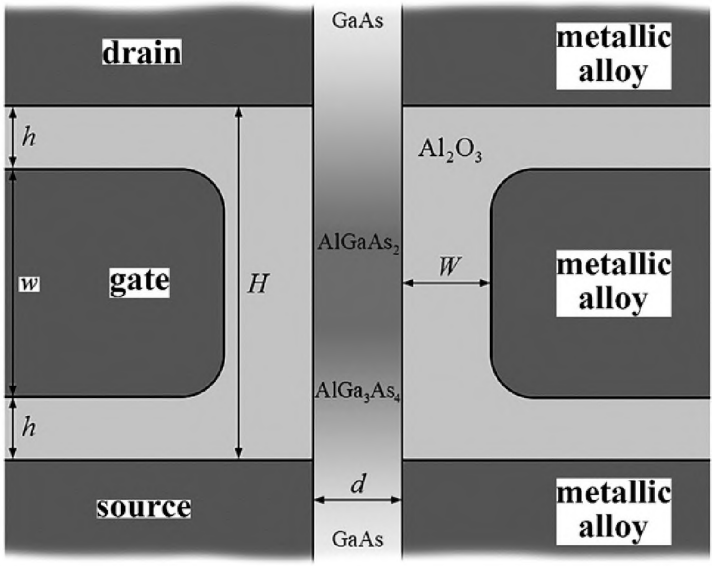

FIG. 1. Cross-section of the transistor by a plane passing through its longitudinal axis of symmetry ($W = 3$ nm, radius of rounding of the gate corner regions is 1 nm) [23, 24]

But in contrast to [23, 24], in which the selection of parameters $d = 10$ nm, $H = 30$ nm, $w = 24$ nm and $h = 3$ nm of a transistor with optimal geometry was justified, a transistor with varying diameter should not have such a short conductive channel. The point is that according to [25], the varying cross section of the semiconductor quantum wire causes the de Broglie waves of electrons to be reflected from regions with varying geometry. To minimize this effect, the changing cross-section region should be as extended as possible. However, in this case instead of the ballistic regime of electron transport in the transistor channel, a quasi-ballistic or even diffusive (diffuse) regime takes place [26, 27] with a sharp drop in the values of channel conductivity and saturation current. In a GaAs quantum wire with a diameter of 10 nm and temperature of 300 K, the average free path lengths for electrons being scattered by polar optical and acoustic phonons are minimal for near-zero kinetic energy of electrons and their energies slightly higher than the polar optical phonon energy (35.5 meV), and according to calculations are respectively about 36 and 28 nm in the regime of current saturation considering the Pauli prohibition principle, the nonparabolicity of semiconductor band structure and the secondary quantum effects. According to [26, 27], if the length of the conducting channel of the transistor is 30 nm or less then almost all electrons transfer through the channel in the ballistic regime. Taking into account all aforementioned, the compromise length of the transistor channel should be of such a minimum possible value, which for the majority of particles from the electron ensemble, on the one hand, corresponds to the transport regime not worse than quasi-ballistic, and on the other hand, as much as possible ensures the accuracy of the Wentzel-Kramers-Brillouin approximation [28] in the quasi-classical description of the one-dimensional longitudinal motion of electrons as much as possible in large regions of the conductive channel of the transistor [29], when one can neglect the reflection of the de Broglie waves from regions with spatially varying potential energy. According to the theory developed in [25], it is enough to increase the length H of the conductive channel of the transistor based on GaAs quantum wire by a factor of 3 to minimize the coherent reflection of most electrons from the classically accessible regions for them in the channel. So it is reasonable to choose

the values of the geometrical parameters of the transistor as follows: $H = 100$ nm, $w = 30$ nm, $h = 35$ nm, $d = d(z)$ ($d_0 = d(0) = d(H) = 10$ nm).

To determine the optimal dependence of the GaAs quantum wire diameter on the z coordinate along its axis ($z = 0$ corresponds to the beginning of the conductive channel of the transistor at the source boundary, $z = H$ corresponds to its end at the drain boundary), it is first necessary to find the distribution of the electric potential $\varphi(r, z)$ in the transistor structure at the defined values of the voltage at the drain ($V_D = 0$) and at the gate V_G (the voltage at the source is assumed to be always equal to zero). It is necessary to calculate the dependence of $\varphi(r, z)$ under such conditions for the following reasons: first, at zero potential at the source and drain, the minimum possible voltage applied to the gate should completely eliminate the potential barrier in the conductive channel of the transistor with the formation of flat subbands and almost unity probability of coherent transfer of electrons through the source-drain region over the entire range of their energy; second, at zero potential at the gate and nominal voltage at the drain, the electric current in the conductive channel of the transistor should be vanishingly small for both transfer of the particles over the barrier and their tunneling through it. These two contradicting requirements can be resolved for some single value of the reference gate voltage V_{G0}. In [22], it was proposed to choose a typical value of V_{G0} equal to 0.5 V for transistors with one-dimensional conducting channels [3, 19, 20]. However, in contrast to [22], according to [23, 24], higher values of electrophysical parameters and electrical characteristics of the nanotransistor can be obtained at a lower value of the reference gate voltage ($V_{G0} = 0.4$ V) due to the consideration of a device with optimal geometrical parameters. Taking it into account, it is reasonable to choose the reference gate voltage equal to 0.4 V.

In the case under consideration, the spatial distribution of the electric potential in the conductive channel of the transistor structure shown in figure 1 can be obtained by numerical solution of the Poisson equation in cylindrical coordinates. In this case, for significant reduction of the computational complexity of $\varphi(r, z)$ calculation, as in [22–24], a number of standard approximations can be applied. First, taking into account a small difference between the values of relative dielectric permittivity of Al_2O_3 [30] and GaAs [31], one can neglect a small jump in the value of the normal component of the electric field strength at the boundary of Al_2O_3/GaAs, which only slightly affects the potential energy of electrons in the electric field through the local displacement of their energy levels in the semiconductor quantum wire. Second, the electric charge of electrons in the conductive channel of the transistor can be neglected. In the closed state of the transistor, neglecting the mobile charge is obviously quite justified. In the open state of the transistor, the maximum possible electric current flowing in its conducting channel, according to the estimates made for the considered geometry of the structure and the position of the Fermi level ($E_F = 0.2$ eV [22–24]) relative to the bottom of the GaAs conduction band in the source and drain regions of the transistor, creates an additional rise in the potential barrier between the source and the gate in the maximum by about 30 mV [22–24]. This results in a shift of no more than 60 mV in the transistor CVC by V_G ($V_G \to V_G + 0.06$ V). Whereas the above approximation frees from the necessity of iterative self-consistent solution of two-dimensional Schrödinger and Poisson equations for each of the calculated points of the transistor CVC. The result of the accepted approximations is the possibility of reduction of the Poisson equation to the Laplace equation in the form of

$$\frac{\partial^2 \phi}{\partial r^2} + \frac{1}{r}\frac{\partial \phi}{\partial r} + \frac{\partial^2 \phi}{\partial z^2} = 0 \tag{1}$$

with corresponding Dirichlet boundary conditions at the Al_2O_3 /"metallic alloy" boundaries, Neumann boundary conditions at the boundary of the modeling domain in Al_2O_3 and at the symmetry axis of the conductive channel of the transistor taking into account that $\varphi \sim r^2$ at $r \to 0$ for any values of z.

After solving the Laplace equation, the electron effective potential energy $u_\varphi(z)$ in an electric field can be estimated by means of standard methods of quantum mechanics, namely in the framework of perturbation theory [20, 32, 33]:

$$u_\phi(z) = -\frac{8e}{d^2(z) J_1^2(\beta_{10})} \int_0^{d(z)/2} \phi(r, z) J_0^2\left(\frac{2\beta_{10} r}{d(z)}\right) r dr. \tag{2}$$

In equality (2), J_n is the Bessel function of the first kind of n-th order, $\beta_{10} = 2.404825558$ [32]. Here, as in other studies [20,22–24,27,32–34], the approximation of the Al_2O_3/GaAs boundary being impermeable for electrons (infinitely high potential barrier) and the approximation of the electric quantum limit are considered. In the latter one, the excited quantum states in Γ valley and quantum states in L and X valleys of the semiconductor quantum wire are not taken into account that in due time was justified in [22–24]. Under the conditions of the electric quantum limit almost all electrons are in the ground quantum state of Γ valley of GaAs. The transverse component of their energy E_0 can be calculated by the formula [20, 22–24, 31, 34–36].

$$E_0(z) = \frac{1}{2\alpha}\left(\sqrt{1 + \frac{8\alpha\beta_{10}^2\hbar^2}{m^* d^2(z)}} - 1\right), \tag{3}$$

where m^* is the effective mass of electron in the GaAs conduction band, α is its nonparabolicity parameter.

Calculation of the optimal dependence $d = d(z)$ under the flat subband condition for the ground quantum state in Γ valley of GaAs at $\varphi_D = \varphi_S = 0$ and $\varphi_G = V_G = V_{G0}$ is carried out by solving the equation [22–24].

$$U(z) = u_\phi(z) + \Delta E_0\left(d(z)\right) = u_\phi(z) + \left(E_0\left(d(z)\right) - E_0\left(d(0)\right)\right) = 0. \tag{4}$$

The numerical solution of equation (4) allows the profile $d(z)$ to be recovered, at which, for a given dependence $u_\varphi(z)$, the flat subband transfer regime is provided for electrons in the ground quantum state of GaAs over the entire length of the transistor channel ($U(z) \equiv 0$). Fig. 2 shows the result of such a numerical calculation for $V_{G0} = 0.4$ V.

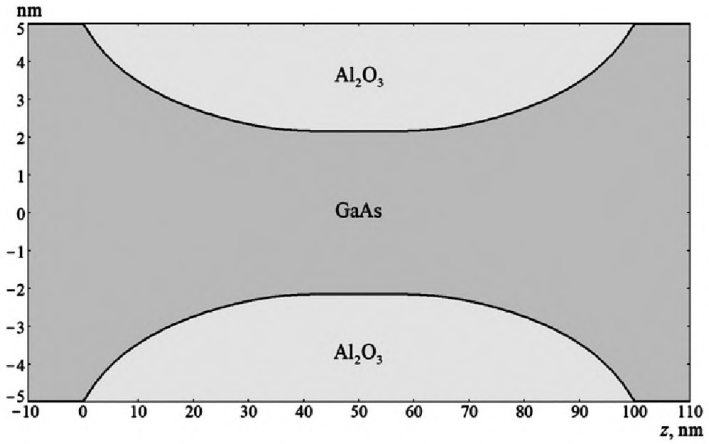

FIG. 2. Optimal dependence of GaAs quantum wire diameter along the transistor channel from the source to the drain

Fig. 3 shows a number of dependences characterizing the electron potential energy profiles lengthwise the transistor channel. In particular, it follows from this figure that, despite the significant voltage applied to the drain, the region of the conductive channel of the transistor near the source is still in the regime of the flat subband due to the screening of the drain field by the gate. At such a shape of the bottom of the semiconductor conduction band in the transistor the electron transfer from the source to the drain is ensured with practically unit probability even at $E \to E_0(0)$.

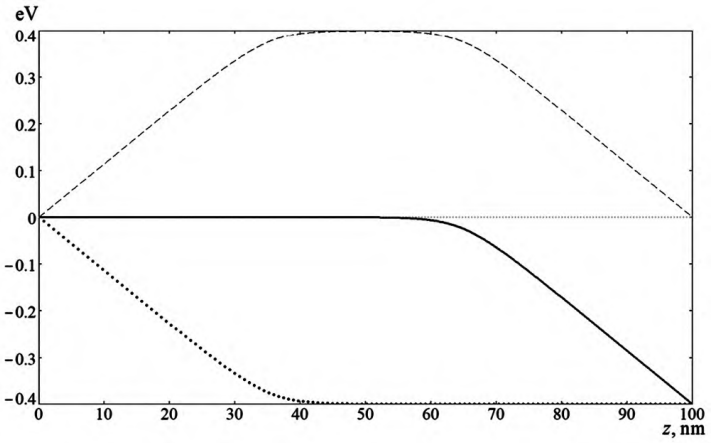

FIG. 3. Variation of electron potential energy profiles along the conductive channel of the transistor from source to drain: dashed curve – potential barrier ΔE_0 in the absence of electric fields ($V_D = V_G = 0$); dotted curve – the potential energy of electrons in the electric field u_φ at $V_D = V_G = V_{G0} = 0.4$ V; solid curve – total potential energy of electrons U at $V_D = V_G = V_{G0} = 0.4$ V

For the considered topology of the transistor structure the calculation of the absolute value of the electric current I_e flowing in the conducting channel can be carried out within the Landauer-Buttiker formalism [14, 21, 22] using the approximation [23, 24].

$$I_e = \frac{e}{\pi\hbar}\int_0^\infty \left(f_{\rm FD}\left(E, E_{\rm F} - E_0(0)\right) t_{\rm sc}^{\rm S}(E) - f_{\rm FD}\left(E, E_{\rm F} - E_0(0) - eV_{\rm D}\right) t_{\rm sc}^{\rm D}(E)\right) t_{\rm ch}(E) dE, \tag{5}$$

where E is the level of electron kinetic energy in the source, t_{ch} is the probability of coherent transfer of electron through the region between the transistor electrodes, $t_{sc}^{S/D}$ is the probability of the electron transfer without scattering through classically accessible regions in the conducting channel from the source (S) or drain (D) side.

To find the value of t_{ch} at a defined value of E, in general, the Schrödinger equation should be numerically solved with appropriate boundary conditions. However, its solution, taking into account the effects of nonparabolicity of the semiconductor band structure, is an extremely difficult problem from the computational point of view [36]. But, taking

into account a number of rigorous generalizations obtained in [36] for the boundary conditions imposed on the wave function when nonparabolicity effects are taken into consideration, it is possible to calculate the dependence $t_{ch}(E)$ in another way, in particular, by means of the transfer-matrix method [34, 37, 38]. For this purpose the entire region from the source ($z = 0$) to the drain ($z = H$) of the transistor is divided into a large number of $Q(q = 0, 1, ..., Q)$ intervals ($z_q - \Delta z/2$, $z_q + \Delta z/2$) of equal width $\Delta z = H/Q$, in each of which the dependence $U(z)$ is replaced by the constant values of $U_q = U(z_q)$ ($\forall f : f_q = f(z_q)$). That is, the dependence of the potential energy of electrons U in the transistor channel on the coordinate z is replaced by its piecewise stepwise approximation U_q. In such a case, applying the transfer-matrix method, the dependence $t_{ch}(E)$ can be rigorously calculated from U_q [36] with much higher accuracy than through the finite-difference approximation of the one-dimensional Schrödinger equation on the same spatial grid $\{z_q\}$ [22–24, 34, 37, 38]:

$$t_{ch}(E) = 1 - \left|\frac{B(E)}{A(E)}\right|^2, \tag{6}$$

$$\begin{pmatrix} A(E) \\ B(E) \end{pmatrix} = \left(\prod_{q=0}^{Q-1} \mathbf{M}_q(E)\right) \begin{pmatrix} 1 \\ 0 \end{pmatrix}, \tag{7}$$

$$\mathbf{M}_q = \frac{1}{2} \begin{pmatrix} \left(1 + \dfrac{m_q^* k_{q+1}}{m_{q+1}^* k_q}\right) \exp\left(-ik_q \Delta z\right) & \left(1 - \dfrac{m_q^* k_{q+1}}{m_{q+1}^* k_q}\right) \exp\left(-ik_q \Delta z\right) \\ \left(1 - \dfrac{m_q^* k_{q+1}}{m_{q+1}^* k_q}\right) \exp\left(ik_q \Delta z\right) & \left(1 + \dfrac{m_q^* k_{q+1}}{m_{q+1}^* k_q}\right) \exp\left(ik_q \Delta z\right) \end{pmatrix}, \tag{8}$$

$$m_q^* = m^* \left(\frac{(E - U_q)^2}{\Gamma_0^2 + (E - U_q)^2}\right)^{1/2} \left(\frac{(E - U_q)^2(\gamma_q + 2\alpha(E - U_q))}{\left(\Gamma_0 + (\Gamma_0^2 + (E - U_q)^2)^{1/2}\right)^2} + \frac{\Gamma_0(2\gamma_q + 3\alpha(E - U_q))}{\Gamma_0 + (\Gamma_0^2 + (E - U_q)^2)^{1/2}}\right), \tag{9}$$

$$\gamma_q = 1 + 2\alpha E_0(d_q) = \sqrt{1 + \frac{8\alpha\beta_{10}^2\hbar^2}{m^* d_q^2}}, \tag{10}$$

$$k_q = \hbar^{-1} \left(\frac{2m^*|E - U_q|(E - U_q)\left(\gamma_q + \alpha(E - U_q)\right)}{\Gamma_0 + (\Gamma_0^2 + (E - U_q)^2)^{1/2}}\right)^{1/2}. \tag{11}$$

In the presented equations, $\Gamma_0 = 10$ meV is a parameter characterizing the average value for the collisional broadening and displacement of the energy levels in the conductive channel of the transistor at temperature $T = 300$ K, which is calculated within the framework of the theory developed in manuscripts [23, 39–42], when considering the scattering of electrons by polar optical and acoustic phonons.

The dependence of $t_{sc}(E)$ can be estimated by Monte Carlo simulation of electron transport in classically accessible regions ($\forall z_q : U_q < E$) [37] applying rather simple algorithm. After casting the value of energy E for an electron injected into the transistor channel according to the Fermi-Dirac distribution function in the source or drain, it is supposed that the particle has overcome the classically accessible regions between the source and drain if during the time of simulation of its motion and scattering, taking into account the occupancy of the final quantum states according to the Pauli prohibition principle, it has achieved the boundary of the potential barrier in the tunneling regime or the boundary of the opposite electrode of the transistor in the case of over-barrier transport. Otherwise, if the electron has left the modeling region, returning back to the injection region, it is considered as reflected particle. To obtain a smooth and stable dependence $t_{sc}(E)$ with respect to the number of simulated particle trajectories, at least approximately 10 million simulation histories should be accumulated.

3. Calculation of the transistor CVCs and discussion of the obtained results

Figs. 4,5 show the results of calculation of the electric current in the conductive channel of the transistor at $T = 300$ K and different values of the voltages on its gate and drain. During the Monte Carlo simulation of charge carriers scattering processes, such electron scatterers as confined polar optical and acoustic phonons were considered according to [39, 41].

The dependencies of electric current in the transistor on the voltage on its drain at specific gate voltages, as illustrated in Fig. 4, are very typical and similar to those observed for conventional MIS-transistors. The current dependencies on the gate voltage at different values of the drain voltage, as presented in Fig. 5, also exhibit a highly characteristic form, corresponding to the pass-through CVCs of conventional MIS-transistors up to the voltage V_{G0}, at which the potential barrier for charge carriers is completely eliminated. But under the condition that $0.5V > V_G > V_{G0} = 0.4$ V, in contrast to the ballistic quantum-barrier transistor which has a plateau on the dependence of $I_e(V_G)$ in this region with negative differential conductivity close to zero, that takes place in case of neglecting the electron scattering processes [22], or positive differential conductivity close to zero, that takes place in case of taking into account these processes [24], the CVCs of the considered quasi-ballistic transistor has no such a valley at $0.4V < V_G < 0.5$ V.

As follows from the simulation results, the maximum saturation current, which is equal to 3.89 μA at $T = 300$ K and $V_D = V_G = V_{G0} = 0.4$, is 56.0 percent of the maximum possible current in the considered transistor (calculated by

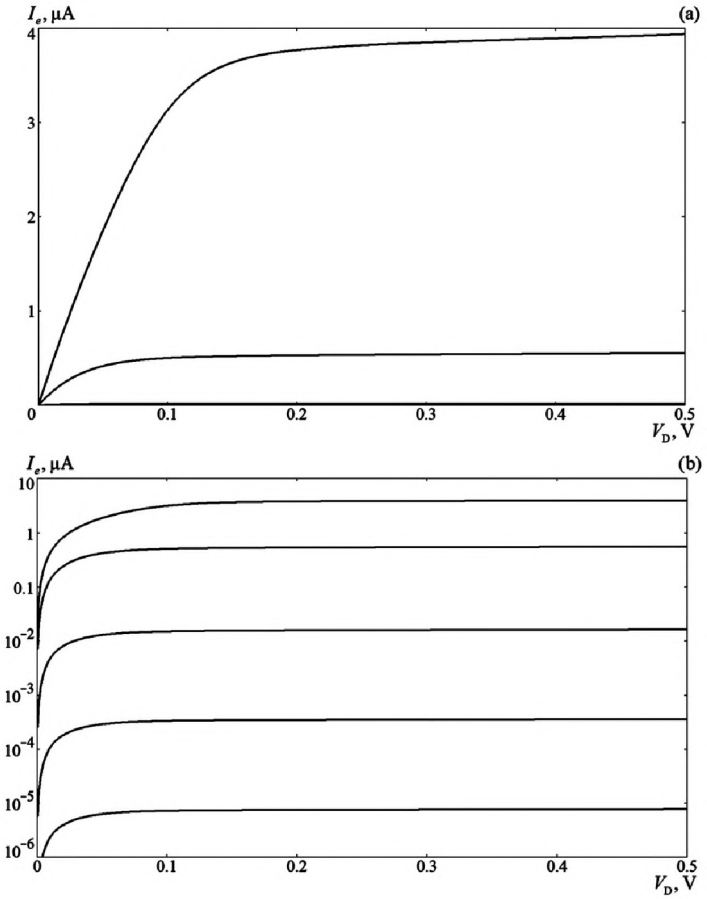

FIG. 4. Output CVC of the FET based on GaAs quantum wire in linear (a) and logarithmic (b) scales: curves in series from top to bottom – $V_G = 0.4$, 0.3, 0.2, 0.1 and 0 V

formula (5) at $V_D \to \infty$ under the condition that $t_{ch}(E)t_{sc}(E) \equiv 1$ [22–24]). The maximum channel conductance of the transistor at $V_G = V_{G0} = 0.4$ V, $V_D = 0$ and $T = 300$ K achieves 55.5 percent of the maximum possible quantum mechanical value of $e^2/(\pi\hbar)$. The ratio of the electric current in the open transistor I_{on} ($V_G = V_{G0}$) to the current in the closed transistor I_{off} ($V_G = 0$) is $5{\cdot}10^5$ at $T = 300$ K and $V_D = 0.2$–0.4 V. At $V_G = 0$ and $V_D = 0.2$-0.4 V the subthreshold swing takes a value of 101 percent relative to the minimum possible theoretical value of ln (10)k_BT/e which is equal to 59.53 mV/dec at a temperature equal to 300 K (k_B is the Boltzmann constant).

When the gate voltage is equal to 0.4 V and more, the transistor conducting channel is completely open due to the complete elimination of the potential barrier for electrons at $V_G \geq 0.4$ V (see Fig. 3,5). Moreover, despite the increase in the fraction of coherently reflected electrons from the region [0, H] of the conducting channel of the quasi-ballistic transistor, there is no typical plateau on CVC of the ballistic transistor at $V_G > V_{G0}$ [22]. The obtained behavior of the pass-through CVC at $V_G > V_{G0}$ is explained by the decrease in the reverse flux of incoherently reflected electrons in the region [0, H], significantly exceeding the increase in the reverse flux of charge carriers coherently reflected from this region. This fact indicates that the conductive channel length of the transistor equal to 100 nm is not optimal and can be reduced with increasing channel conductivity and saturation current along with increasing the subthreshold swing to values not worse than 105% relative to the minimum possible theoretical value [22–24]. In particular, basing on the results of the present study and the results from [22–24], it can be concluded that the optimum value of h_0 satisfies the inequality chain like $3 < h_0 < 30$ nm. Obviously, the optimum will be achieved when the backward flux of electrons incoherently reflected by phonons is equal to the backward flux of particles coherently reflected from the surface of the quantum wire which tapers sharply along its axis [25]. Unfortunately, within the approach considered in the present study, it is not possible to find the optimal value of h_0 in terms of the maximum channel conductance or maximum saturation current. To obtain a relevant optimal value of h_0, it is necessary to use much more rigorous and computationally very complex methods for calculating the electric current in one-dimensional conducting channels with complex topology and decaying electron quantum states because of decoherence processes [43–45]. Here, we can only assume that $h_0 \sim 10$ nm ($H_0 \sim 50$ nm).

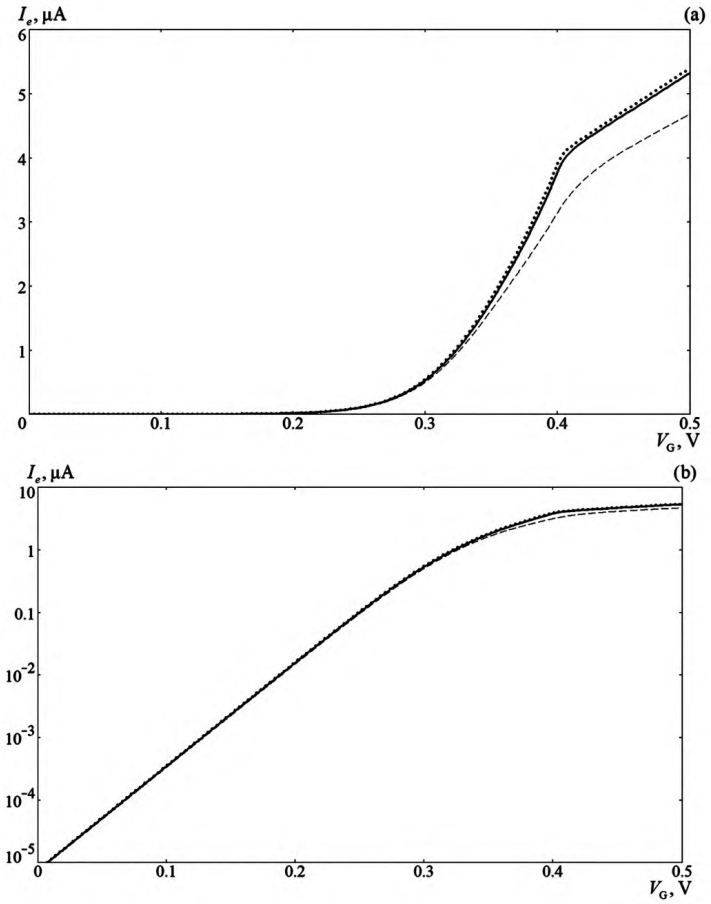

FIG. 5. Pass-through CVC of the FET based on GaAs quantum wire in linear (a) and logarithmic (b) scales: dashed curve – $V_D = 0.1$ V, solid curve – $V_D = 0.2$ V, dotted curve – $V_D = 0.4$ V

4. Conclusions

Thus, within the framework of the present study, a topological solution for a new construction of FET with a Schottky barrier in its conductive channel in the form of a quasi-ballistic quantum-barrier transistor based on a cylindrical undoped GaAs-in-Al_2O_3 quantum wire with an optimally varying cross-section lengthwise the conducting channel has been found. The CVCs of such a transistor have been calculated within the framework of the developed combined physico-mathematical model describing electron transport in its conducting channel taking into account the semiconductor band structure nonparabolicity, quantum-dimensional effects and such secondary quantum effects as the collisional broadening and displacement of the electron energy levels.

The proposed solution, among other things, opens the prospect of development and production of quantum-barrier FETs based on semiconductor quantum wires with varying rectangular cross-section lengthwise the conducting channel along one or both transverse directions. In the limit, it could be a semiconductor quantum layer with optimally varying thickness lengthwise the two-dimensional conducting channel of the transistor separated from two planar metal gates by some oxide or nitride insulator. As an example, it could be such a heterostructure as "metal/SiO_2/Si[111]/SiO_2/metal". Orientation of the semiconductor along the [111] direction perpendicular to the heterojunctions is necessary to ensure the same position of the lowest energy subbands in all six valleys of silicon relative to the bottom of its conduction band. When changing the Si quantum layer thickness from 4.8 nm (15 atomic layers) through 1.6 nm (5 atomic layers) to 4.8 nm (15 atomic layers), a profile of the potential barrier for electrons is formed close to the optimal profile obtained in the present study.

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Information about the authors:

Dmitry V. Pozdnyakov – Belarusian State University, Minsk, Nezavisimosti Av.4, 220030 Belarus; ORCID 0009-0005-2333-9829; pozdnyakovdv@bsu.by

Andrei V. Borzdov – Belarusian State University, Minsk, Nezavisimosti Av.4, 220030 Belarus; borzdovav@bsu.by

Vladimir M. Borzdov – Belarusian State University, Minsk, Nezavisimosti Av.4, 220030 Belarus; borzdov@bsu.by

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