ISSN 1063-7397, Russian Microelectronics, 2021, Vol. 50, No. 1, pp. 63–68. © Pleiades Publishing, Ltd., 2021.
Russian Text © The Author(s), 2021, published in Mikroelektronika, 2021, Vol. 50, No. 1, pp. 68–73.

Effect of Process-Related Impurities on the Electrophysical Parameters of a MOS Transistor

V. B. Odzhaev[a], A. N. Petlitskii[b], V. S. Prosolovich[a, *], V. A. Filipenya[b], V. Yu. Yavid[a], and Yu. N. Yankovskii[b]

[a] *Belarusian State University, Minsk, 220030 Belarus*
[b] *OAO INTEGRAL, Management Company of INTEGRAL Holding, Minsk, 220108 Belarus*
**e-mail: prosolovich@bsu.by*

Received May 8, 2020; revised May 14, 2020; accepted July 2, 2020

Abstract—It is established that the electrophysical characteristics of MOS transistors largely depend on the quality of a gate dielectric. The presence of an extra built-in charge in the dielectric and fast surface states at the SiO_2/Si interface leads to both an increased threshold voltage and decreased saturation current and voltage, decreased slopes of the characteristics of the MOS transistor in the linear and saturation regions, and a decreased structure conductance in the linear region. The gate leakage currents also increase. It is shown that the view and shape of the capacity–voltage characteristics are determined by the value of an extra positive charge in the bulk of the dielectric and the density of fast surface states at the Si/SiO_2 interface. These values are correlated to the profile of the distribution of the surface concentration of the process-related impurities adsorbed at the wafer surface during the manufacturing of the device, which allows us to judge the quality of the materials used, adherence to the production conditions, and, if necessary, correct them opportunely as required.

Keywords: MOS transistor, dielectric, surface states, leakage current, interface
DOI: 10.1134/S1063739720060086

INTRODUCTION

In the production of CMOS structures, a large number of production steps are required, especially when MIS technology is used [1–3]. Manufacturing quality control is a constituent part of the typical manufacturing process and is reduced to the determination of two components: obvious defects characterizing the yield of the device and latent defects reducing their reliability. The aim of the production control is not only to obtain the desired quality of devices but also to timely reject the defective items at different steps of the production of the device.

The choice of the chemical reagents and assignment of such a sequence of production operations, in particular, high-temperature ones, which would preclude uncontrolled (process-related) impurities falling into a semiconductor structure as far as possible, is critically important. The changes in the parameters of a manufacturing process, taking place as the characteristic size of a transistor becomes smaller, should not lead to a decrease in the yield of the device.

As a result of this, revealing the reasons for the labile reproducibility of the main characteristics of MOS transistors in order to establish the factors determining the reliability and stability of the performance of integrated microcircuits is a topical task. One of the reasons for the degradation of the electrophysical parameters of MOS transistors is the contamination of a silicon substrate with process-related impurities during the manufacturing process. To check these suppositions, we investigated the MOS structures using the technique of current–voltage (I–V) characteristics and high-frequency capacity–voltage (C–V) characteristics, and measured the concentration of the process-related impurities both on the surface and in the bulk of silicon wafers.

OBJECTS AND METHODS OF RESEARCH

Using an Agilent B1500A semiconductor device parameter analyzer with a Cascide Summit11000 probe station, the I–V and C–V characteristics of two batches (A and B, hereinafter) of n-channel MOS transistors produced via the same process routes with the same process materials, but at different times, were measured. Pockets of MOS transistors 70 × 70 μm in size were created on p-type silicon wafers with a resistivity of 10 Ω cm by ion-implantation doping with boron (BF_2) for the p pocket, and phosphorus and arsenic doping for the n pocket. The size of a polysilicon gate of a transistor doped to degeneracy was 10 × 10 μm. The gate dielectric's (SiO_2) thickness was