A NEW TECHNOLOGY OF FABRICATING OHMIC METAL-SILICON CONTACTS

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Results of performing dry cleaning, doping of silicon in BF_3+H_2 and BF_3+H_2+CF_4 plasma during fabrication of ohmic constants in equipment having the same hardware configuration have been considered based on the concept of a closed manufacturing system.

Introduction

Ultra clean technology (ultra clean processing environment, ultra clean wafer surface, perfect process parameter control) is a crucial factor in developing high-quality processing technology for future VLSI fabrication [1,2].

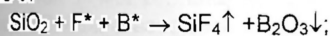
In the previous articles the critical problems required for high quality processing for VLSI manufacturing were discussed in detail based on experimental data and models of the processes using support of charges on the surface of semiconductor p – (n) – type in contact with plasma [3,4].

The aim of the present work is to study the effect of dry cleaning and doping of Si wafer in (BF_3+H_2) and (BF_3+CF_4+H_2) plasma on the contact resistance of Mo/p^+ – silicon contacts.

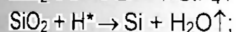
I. Experimental

The films of Mo were made using a model УПР–1 production plasma sputtering system. The films were deposited in the following way.

First, wafer are etched by F*, H* (BF_3+H_2 or BF_3+CF_4+H_2) plasma in the vacuum chamber at the pressure of (5 – 6) $\cdot 10^{-2}$ Pa, and the potential of 30 – 150 V.



$SiO_2 + F^* + B^* \rightarrow SiF_4\uparrow + B_2O_3\downarrow$;



$SiO_2 + H^* \rightarrow Si + H_2O\uparrow$;

Addition of CF_4 is known to provide reduced doping of silicon by B and decreased lattice imperfections density.

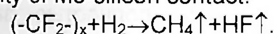
Second, wafer are doped by B and at the same time are covered by Mo at the potential of target equal to 2-3 kV.

II. Results

We have found that the Mo/p^+ silicon contact resistance was reduced by the process in which wafer are etched in the mixture of 75%BF_3+25%H_2 and 55%BF_3+20%CF_4+25%H_2 (Table, processes 4, 5).

Dry cleaning, doping of silicon by B and cathode sputtering of Mo in a closed manufacturing system in which wafers go through all fabrication processes in isolation from the air reduce the Mo/p^+ silicon contact resistance to 0,02 Ω (process 4) and to 0,01 Ω (process 5) as compared with the processes 1,2,3 [4],6 [2].

In our processes the presence of H_2 in plasma prevents formation of polymer film $(-CF_2-)_x$ making worse the quality of Mo-silicon contact:



$$(-CF_2-)_x + H_2 \rightarrow CH_4\uparrow + HF\uparrow.$$

Reducing of BF_3 in BF_3+H_2+CF_4 plasma has no effect on decreasing F*, because CF_4 is their source, that is why the rate of cleaning of contact windows and its quality are not lowered.

Moreover we have found that the SiO_2/Si etching selectivity in plasma (process 5) is 6 times higher than that in CF_4 plasma (process 2). The mechanism of drastical reducing of contact resistance Mo-Si is discussed.

Table
The effect of treatments of Si wafer on the contact resistance of Mo-Si system

Process	Treatment Type	Contact Resistance Mo/p^+Si, Ω
1	Without treatment, only cathode Mo sputtering in Ar plasma	0.40
2	a) Dry cleaning at plasma CF_4; b) Cathode Mo sputtering in Ar plasma	0.27
3	Dry cleaning, doping and cathode Mo sputtering in BF_3 plasma	0.10
4	Dry cleaning, doping and cathode Mo sputtering in BF_3+H_2 plasma	0,02
5	Dry cleaning, doping and cathode Mo sputtering in BF_3+H_2+CF_4 plasma	0,01
6	a) Wet chemical cleaning in H_2O_2 :NH_4OH : H_2O = 3:3:7 b) Heating to 550K, annealing for 40 min, pressure of $1\cdot10^{-4}$Pa c) Wet chemical cleaning in H_2O_2 :NH_4OH : H_2O = 3:3:7 d) Wet chemical cleaning in 1% HF	0,07

Conclusion

It appears that the application of new technology for fabrication of ohmic contacts to silicon makes it possible to develop a high-quality process technology for semiconductor devices fabrication.

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