

# INTEGRATED CIRCUIT (IC) AND PHOTOMASK IMAGES PROCESSING TECHNOLOGY

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**Abstract.** The integrated circuit and photomask images processing technology is proposed. This technology allows to perform the restoration of the integrated-circuit metallization layout and the mask artwork from the images of IC metallization layers or photomask set correspondingly. It can be applied for the tasks of integrated circuits redesign and automated visual inspection of integrated circuits and photomask production.

## 1. Introduction

The modern semiconductor manufacturing needs to control all of the critical process modules that drive IC manufacturing success. Several factors inherent in the semiconductor industry drive the critical need for comprehensive yield management and process control solutions. Among the most significant of these are: increasing device complexity; shrinking geometries; reduced product life cycles. The visual or optical inspection is the important part of such control solutions. It implies the presence of some operative analysis system [1] providing image registration, visual information processing and analysis. In this paper the main attention is paid to image processing technology which was developed for this sort of the systems.

## 2. Problem formulation

The proposed technology has the following objectives: 1 restoration of the integrated-circuit metallization layout from the images of IC metallization layers; 2 restoration of the mask artwork from the images of photomask set. Thus, the objects of processing are raster patterns of IC metallization layers and IC photomasks, represented as the collection of partially overlapping images (frames) without any reference marks (Fig 1.). In the case of IC-metallization restoration it is required to represent this pattern in the vector format for reproduction of connection layout. The second goal implies representation of the mask artwork pattern in the vector format for technological rules inspection and, if necessary, to correct a vector description according to these rules. Therefore, the IC and photomask design rules should be considered during the restoration process.

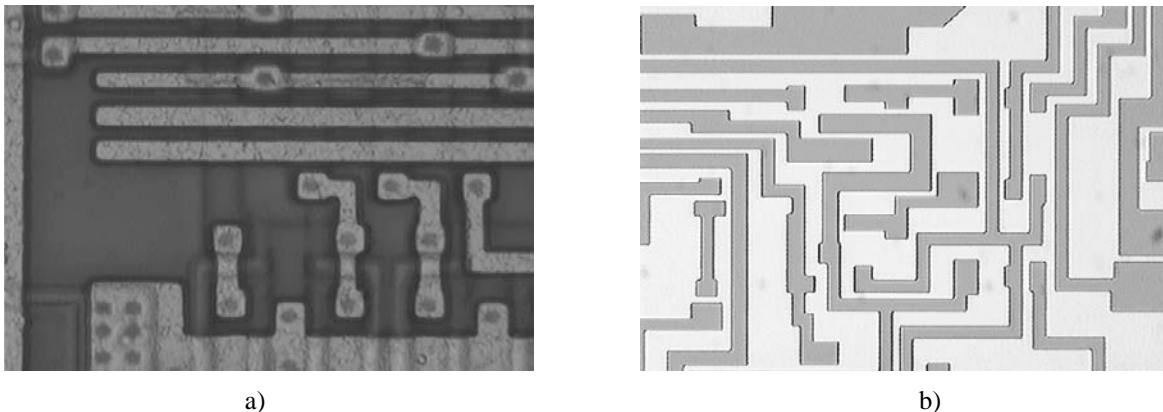


Fig.1. a) IC metallization layers, b) IC photomasks

## 3. Design rules

Mead and Conway formulated the main principles of IC topology design for MOS ICs [2]. We shall consider ICs manufactured under MOS technology that nevertheless does not restrict of generality of the proposed technology. Consider the following constraints for a layer:

**K** - minimal size of bonding contact pad

**R** - minimal distance from a bonding contact pad to the metal conductor;

**S** - length of side;

**S1** - width of the ring of a bonding contact pad;

**R1** - minimal distance between metal conductors;  
**D** - minimal metal conductor width.

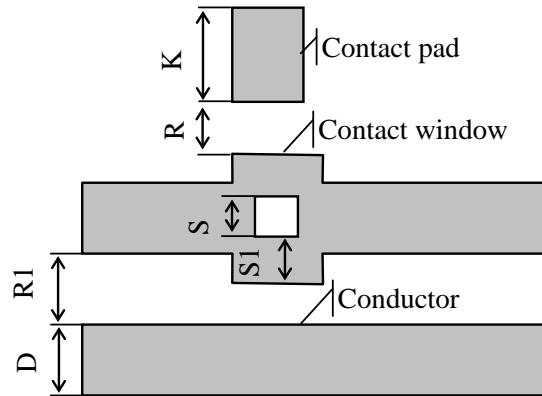


Fig 2. The example of some design rules for metallization layer

There is the only one restriction for neighbouring layers - maximal displacement between centres of the same contact windows.

#### 4. The main image processing and image analysis algorithmic stages

The technology includes the following image processing and image analysis algorithmic stages (Fig. 3). Consider each stage in more detail.

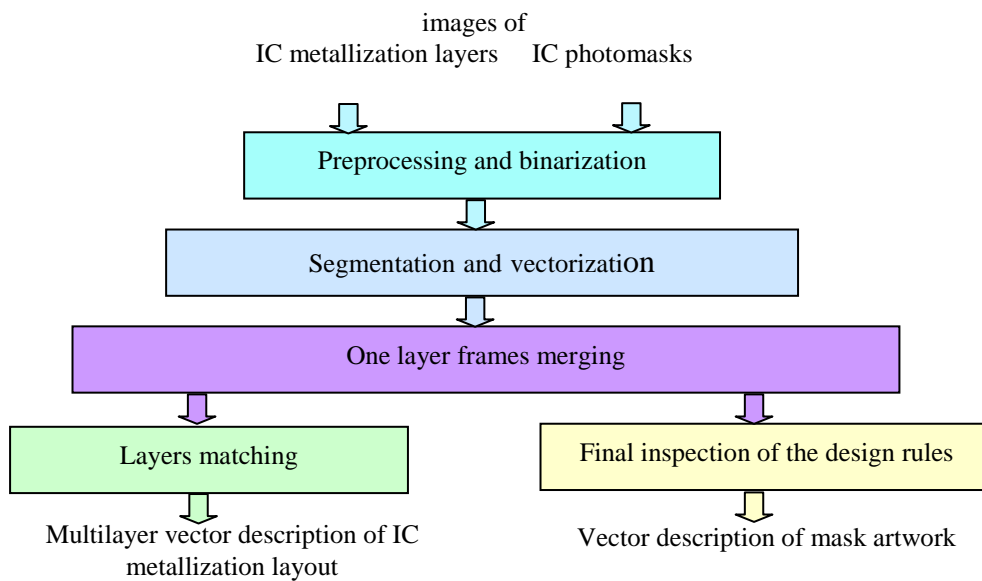


Fig. 3. Basic algorithmic stages

The images of IC metalization layers or IC photomask are entered into the **preprocessing and binarization** stage, which includes the following operations [3]:

- filtration with the antialiasing purpose and noise removal in the frequency domain;
- image thresholding (binarization);
- improvement of image quality by removal of blobs and aligning of boundary lines.

The last step is performed considering design rules on the base of spatial filtering methods and operations of mathematical morphology. The configuration and size of the mask for spatial filters, number of dilatation / erosion iterations are selected on the basis of the following layer constraints: **D**, **R** and **R1**. The result of preprocessing and binarization is shown in Fig. 4

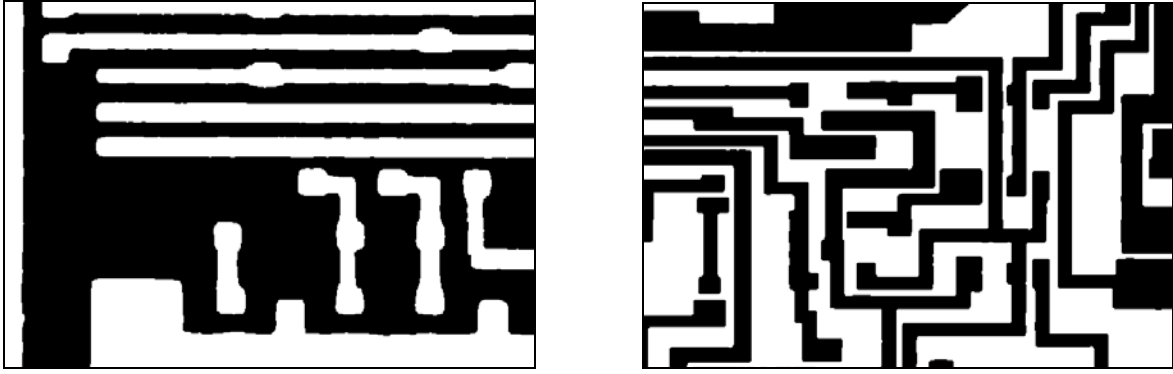


Fig. 4. Images after preprocessing and binarization stage

The stage of **Segmentation and vectorization** includes the following operations [4]:

- Object contour extraction.
- Extraction of straight lines which approximate binary contours on the basis of Hough transform. The preliminary consideration of technology constraints: **D**, **K**, **R** and **R1** is performed by means of variation of Hough transform parameters such as: the orientation of the extracted lines, minimum number of points located on the extracted line, minimum distance between lines.
- Searching cross points of straight lines. These points are “candidates” pointing the change of boundary direction.
- Creation of an “elementary” region set covering the initial image on the base of retrieved points.
- Merging the one-type neighbouring regions into the ultimate area.

The result of segmentation and vectorization is shown in Fig. 5.

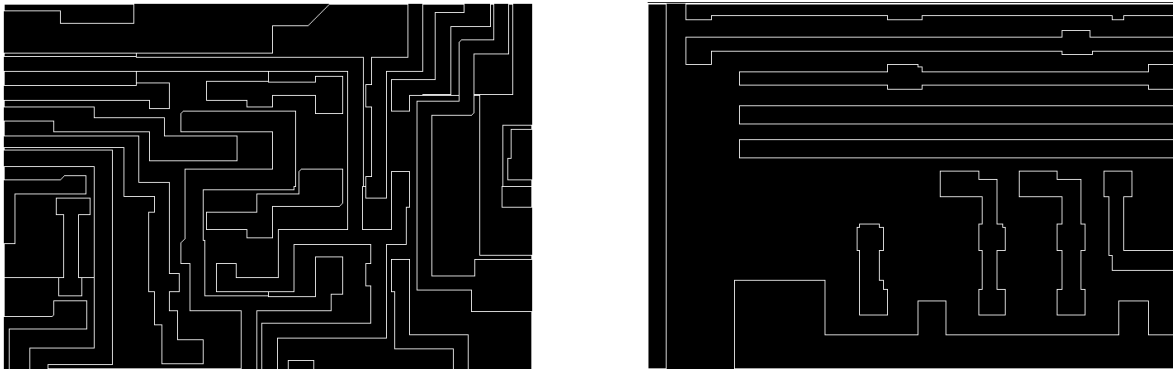


Fig.5 The result of segmentation and vectorization

**One layer frames merging** is performed to obtain a single vector description of one metallization layer or one photomask and final inspection of design restrictions **D**, **K**, **R**, **R1** for them. This problem is non-trivial due to registration equipment mistakes: perspective distortion, blurring, shifting and so on.

The algorithms of quasi-optimal picture areas matching [5] have been developed for this task. The result of frame merging is shown in Fig.6.

**Layers matching** is necessary for the correction of displacements in the final multi layer description of the object. It is performed by means of corresponding contact pads connection. The following operations are performed:

- Creation of the library of bonding contact pad patterns.
- Detection of the bonding contact pads for each layer by using correlation or neural network techniques. Additional inspection of the **S** and **S1** constraints is performed during this stage.
- Connection of corresponding contact pads from neighbouring layers.
- Detection of missed or redundant contact pads.

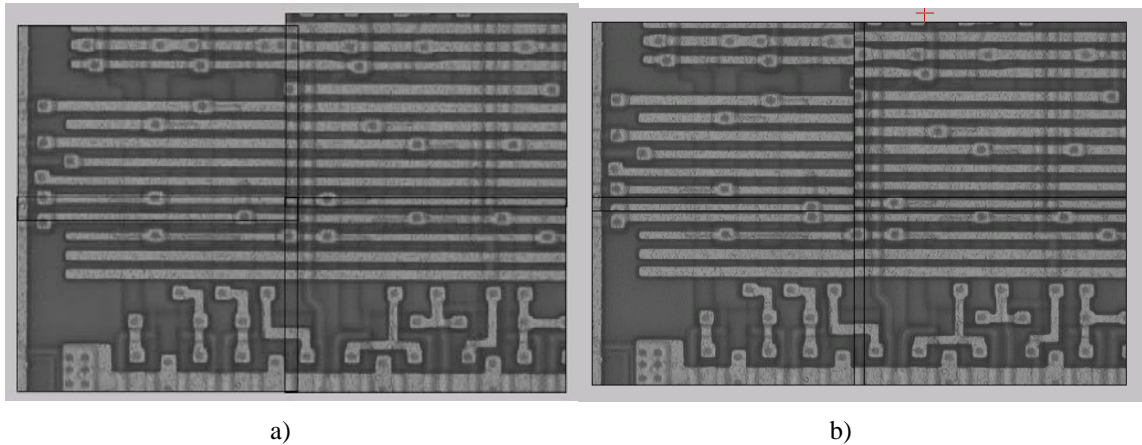


Fig. 6. a) the collection of four frames, b) the result of frames merging

**Final inspection of the design rules.** On this stage special inspection algorithms process the obtained vector description of the mask artwork and perform the final inspection of all design rules and defect localization. The sample of detected defects is shown in Fig. 7.

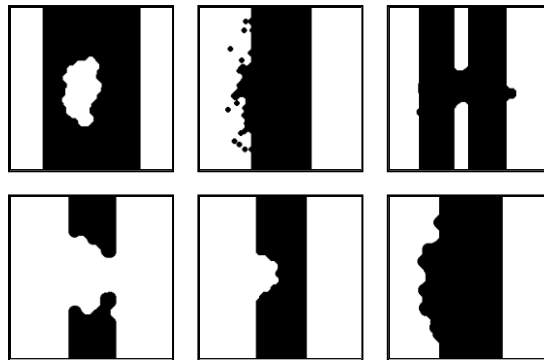


Fig. 7. The sample of defects

## 5. Conclusion

Proposed technology was tested by applying its to the task of restoring ICs metallization layout. Thus the localization of defects has not been produced, but the automatic image correction has been performed. The high-quality restoration of explorers and bonding contact pads was reached at processing of the colour and grayscale images with two spectral gradations.

Further investigations envisage the modification of the technology for analysis of diffusive and active component IC layers and restoration of the whole IC layout. The technology can also be spread to the printed circuit boards processing.

## References

- [1]. Voganti, F. Ercal, C. Dagli, S.Tsunekawa. Automatic PCI Inspection Algorithms: A Survey, *Computer Vision and Image Understanding*, **63**, (1996), 287-313.
- [2]. C. Mead, L. Conway, eds. Introduction to VLSI Systems, *Addison-Wesley*, 1980.
- [3]. Doudkin A.A., Vershok D.A., Sadykhov R.Kh., Selikhanovich A.M. Contour extraction algorithm for LSI circuit video image processing. *Proc. of the Int. Workshop (IDAACS'2001)*, Foros, Ukraine, 1-4 July 2001, 69-72.
- [4]. Vershok D.A. The algorithm of segmentation of grayscale images. *Proc. of the 2nd int. conf. (ICN-NAI'2001)*, Minsk, Belarus, 2-5 oct. 2001, 143-146
- [5]. Doudkin A.A., Sadykhov R.Kh., Vatkin M.E. The Algorithms of Quasi-Optimal Picture Areas Matching. *Proc. of the Second IEEE Int. Workshop (IDAACS'2003)*, Lviv, Ukraine, 8-10 September 2003, 214-217.
- [6]. Doudkin A.A., Vershok D.A. Computer-Aided Inspection of Some Design Rules of Integrated Circuit Layers. *Proc. of the Second IEEE Int. Workshop (IDAACS'2003)*, Lviv, Ukraine, 8-10 September 2003, 232-235.