ГРАФОВЫЕ МОДЕЛИ ДЛЯ ОЦЕНКИ ЭЛЕКТРОПОТРЕБЛЕНИЯ ЛОГИЧЕСКИХ СХЕМ

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Изучается проблема оценки прогнозируемой мощности, потребляемой последовательными CMOS-схемами, с использованием моделирования. Рассматривается задача формирования тестовых последовательностей входных воздействий для оценки средней активности выключателя цепи. Предложены графовые модели последовательных схем, позволяющих формализовать процесс генерации тестовых последовательностей.

Ключевые слова: CMOS-технология; рассеиваемая мощность; активность по переключению.

GRAPH MODELS FOR ESTIMATION OF POWER CONSUMPTION OF LOGIC CIRCUITS

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The problem of estimation of the projected power, consumed by the CMOS sequential circuits, by means of its simulation is discussed. The task of forming test sequences of input actions to estimate the average circuit switch activity is considered. Graph models of sequential circuits allowing to formalize the process of generating test sequences are suggested.

Keywords: CMOS technology; power dissipation; switching activity.

INTRODUCTION

In the last years power consumption has become the major issue in electronic research, it is being given increased weight in comparison to area and speed cost which were historically the major considerations in VLSI circuit design. Excessive power dissipation in integrative circuits causes their overheating, degrading the performance and reducing chip life. The Semiconductor Industry Association technology roadmap [1] has identified low power design techniques as a critical technological need in semiconductor industry today. Accurate and efficient power estimation during design phase is required. The appropriate tools must have efficient means to estimate the power consumed by a circuit on different design phases. At present an increasing attention is focused not only on transistor-level design but on higher
levels of abstraction because early power estimation is important in VLSI circuits, because it has a significant impact on the reliability of the circuits under design. In the process of optimizing circuits for low power a designer is interested in knowing the effects of specific design techniques on the power consumption of the projected circuit. With the relevant information about power characteristics designer can redesign or correct a circuit in early design stages if it can consume more power than expected.

Currently, the simplest and most direct power estimation can be done by circuit simulation when the monitoring of the power supply current is done. Power consumption values are determined which depend on the given vector set. So, using simulators, power is measured for a specific set of input vectors (often chosen randomly) referred to as test sequence.

Power and switching activity estimation for sequential circuits is significantly more complex task than that for combinational circuits because power value depends not only on input patterns but on the state the circuit is in. Although the problem of estimation of power in VLSI circuits is essential for determining the appropriate packaging and cooling techniques, optimizing the power and ground routing networks, there are a limited number of papers devoted to the problem of average and maximum power estimation of sequential circuits.

In the paper the task of average switching activity estimation for CMOS synchronous sequential circuit is considered when its automaton description in the form of Finite State Machine (FSM) is available. The methods are based on finding out directed paths of special type for proposed graph models generated by FSM state transition graph (STG). The paths are closely related with input patterns for simulating the sequential circuit for power estimation.

**BASIC DEFINITIONS AND PROBLEM STATEMENT**

For adequate estimation of energy consumption a large number of input actions (allowing to make statistically significant conclusions) should be considered with this test sequence should correspond to a normal mode of test circuit operation. If the conditions of the circuit use are not known, the most effective toll will be pseudo-random test sequence of the exhaustive search, which must include every possible ordered pair of inputs (from the Boolean space of dimension \( n \), where \( n \) is the number of the circuit inputs), and adjacent elements in it will be presented exactly once. The minimum size of such a test sequence is \( 2^n (2^n - 1) + 1 \) \[2\]. This estimate, however, can be achieved only in the case of combinational circuits. For circuits with memory, this problem is much more complicated, since it is necessary to take into account changes in the state of the memory elements and their attainability during sequential circuit operation.

At the level of logic design a gate-level netlist is generated from a FSM, so a circuit operation is reflected by an appropriate FSM structure. We make an assumption that the sequential circuit automaton description in the form of FSM state transition graph (STG) is available. We seek for test sequence of input vectors that are the candidates to be tested for the average power dissipation in sequential circuit. The test sequence is derived from augmented STG of the given FSM.

STG is a directed graph whose vertices correspond to the automaton states \( s_i \), and its arcs – to transitions between the states. Any arc of the graph is marked with the set \( x_{ij} \) of input symbols (a set of values of input variables \( x = (x_1, x_2, \ldots, x_n) \)) which cause the corresponding transition from the state \( s_i \) into \( s_j \). It is assumed that the automaton STG is strongly connected, i. e. for any pair of states always exists a sequence of input signals that brings the automaton from the one state to another. Figure 1 shows an example of such a STG, each arc of the graph is labeled by a pair: the arc number/the set \( x_{ij} \).
Let \( T_i \) denote test sequence in the form \((s^i, x_1^i, x_2^i, \ldots)\), where \( s^i \) is a FSM internal state represented by a Boolean vector of memory elements states, \( x_j^i \) is a Boolean vector of input variable values representing a FSM input state at the \( j \)-th clock cycle. The values of \( s^i \) and \( x_1^i \) initialize the circuit at the first clock cycle, before the process of estimating the series of switching’s in the circuit. During a circuit simulation under the test \( T_i \) the sequence \((s^i, x_1^i, s_1^i, x_2^i, s_2^i, \ldots)\) of automaton states changes is generated.

When simulating the circuit to estimate its average energy consumption it is desirable to analyze its responses to every possible change of its inputs. So, it is advisable to consider all possible ordered pairs of input combinations that are valid at the normal mode of the circuit functioning. When testing sequential circuit, input patterns following one after another are separated by different states of memory elements. In other words, it is necessary to test not only pairs but various three elements fragments \((s^i, x_1^i, x_2^i)\) which are allowable by the given automaton STG. For example, the arc 7 (fig. 1) corresponding to the transition with the input condition \( x_1 \bar{x}_2 \ (10) \) is immediately preceded with the arcs 9 or 11 (corresponding to automaton transitions into the state \( s_3 \)), i.e the test sequence should include three elements fragments \((s_4, \bar{x}_1 \bar{x}_2, s_3, x_1 \bar{x}_2)\) and \((s_5, x_1 \bar{x}_2, s_3, x_1 \bar{x}_2)\) corresponding to pairs of 9, 7 and 11, 7.

![Fig. 1. Automaton state transition graph](image)

The test sequence \((s^i, x_1^i, s_1^i, x_2^i, s_2^i, \ldots)\) for calculating the energy consumption of a circuit implementing an automaton description should satisfy the following conditions:

1) the internal state \( s^i \) should be reset state as any test scenario can run from the test circuit reset state;

2) the test sequence should consist of alternating input patterns and automaton internal states, which are provided by a traversal of all the arcs of the STG (not necessarily once), starting with a given internal state \( s^i \);

3) the test sequence should include every possible triple mentioned above.

The existence of such a sequence \((s^i, x_1^i, s_1^i, x_2^i, s_2^i, \ldots)\) is provided by the assumption that an automaton STG is strongly connected. The question is how to find it in an efficient manner.

**GRAPH MODELS TO SEARCH TEST SEQUENCE**

The input data for generating the test sequence is a connected directed graph \( G = (V, E) \) corresponding to the initial automaton STG. It is multidigraph that may have multiple arcs and sometimes loops.

It would seem, the task of forming the test sequence could be reduced to searching the shortest directed walk (as an open finite alternating sequence of vertices and arcs) that visits each arc in \( G \) at least once. The the task can be stated as the Chinese postman problem for
the case of digraphs: given a directed graph, find the shortest closed walk that visits all the arcs at least once. Indeed, the traversal of every arc of the multidigraph is the necessary condition, but since one of the defining feature of an automaton model is that there is typically a large number of possible «next actions» at every vertex in the graph \( G \) and we would like to test these combinations too. The Chinese Postman (and its variations) solutions guarantee visiting every arc, but not every arc combination of the length 2. The last demand is greatly difficult to perform solving the Chinese Postman problem on the graph \( G \).

The idea of the proposed solution of the problem consists in the use of another automaton graph model, which allows easy to deal with combinations of the length 2 of arcs of the graph \( G \). Such a graph model proves to be the line graph \( L(G) \) of the graph \( G \). The vertexes of the line graph \( L(G) \) [3] correspond to the arcs of \( G \) and \( L(G) \) represents the adjacencies between arcs of \( G \). If \( G \) is a digraph, its line graph is directed too. Line digraph \( L(G) \) has one vertex for each arc of \( G \). Two vertices representing directed arcs from \( p \) to \( q \) and from \( u \) to \( v \) in \( G \) are connected by an arc from \( pq \) to \( uv \) in the line digraph when \( q = u \). That is, each arc in the line digraph \( L(G) \) represents a length-two directed path in \( G \) (or a pair of automaton transitions).

Fig. 2 shows the line graph \( L(G) \) for the graph \( G \) (fig. 1). Each vertex of \( L(G) \) is shown labeled with the label of the corresponding arc of \( G \).

![Fig. 2. Line graph L(G)](image)

Thus, if to find such a walk in the digraph \( L(G) \) that passes through all its arcs at least once, the task of finding a test sequence to estimate the average power dissipation of the sequential circuit will be solved. The walk should begin with one of the arcs proceeding from the initial automaton state (reset state) that is zero encoded. For our example, this arc may be the arc 1. The desired test sequence \((s_1, x_1', x_2', x_3', ...)\) will consist of input patterns assigned to passable vertexes of the line graph \( L(G) \) (corresponding to arcs of the digraph \( G \)).

**THE WAYS OF SEARCHING THE TEST SEQUENCE**

As stated above the problem is to find the shortest walk in digraph \( L(G) \), which passes through each digraph arc at least once.

Here we consider three approaches to the problem solving.

1. **Optimal walks.** It is clear that the minimum walk length is achieved when each arc is traversed exactly once. Such a decision might take place in the special case when \( L(G) \) is Euler graph (scarce graph type). In other cases, the desired walk will contain repeated arcs.
The goal is to minimize the number of repeated passages of arcs. The solved problem is similar to the problem of the Chinese postman and its variation for digraphs – the New York Street Sweeper Problem [4] (the difference: it is not necessary to obtain a cycle and the weights of all arcs are equal).

But it is well known that Chinese postman problem is hard. So, there appears a modest chance to find such a solution for digraphs of high dimension. As is easy to see, each vertex of degree $k$ in the original graph $G$ creates $k(k−1)/2$ arcs in the line graph $L(G)$. This means that transforming a “thick” graph into a line one results in considerable increasing its complexity.

2. Random walks. A random walk consist in wandering round the digraph $L(G)$ from the initial vertex. At each repeating step of the process, choose at random an outgoing arc from the current vertex, then follow that arc to the next vertex. Random walk is very simple to implement for graphs of great complexity. The disadvantage of random walk method is its inefficiency: they tend to re-traverse some arcs and does not traverse some others.

3. Guided walks. It would be helpful if the random walk is guided to be in area of more interest. First of all, it can look what arcs were passed and try to choose during random walk preferably those arcs that were not traversed. Then, the arc choice at each step with taking into account the probabilities of the appropriate automaton transitions more powerfully promotes the efficiency of the process of forming test sequence. So, we can provide the random walk that will be biased toward the transitions that the automaton is more likely to perform.

The guided walks of the last type can be organized when for every circuit input we know the probability that it will be in the state 1 in any circuit operation cycle. Knowing such values, we can calculate the probabilities of automaton transitions [5] and assign the values to corresponding arcs of the digraph $G$ obtaining digraph with weighted arcs. Its line digraph $L(G)$ will be digraph with weighted vertexes.

So, the process of random walk should be organized to guide the random walk such a manner that it will be statistically more likely to follow the higher probability vertexes. In each step of the guided walk, the probability of an arc choice should be proportional to the probability of a vertex the arc will enter.

CONCLUSION

The suggested graph models are an excellent instrument to solve the problems of generating test sequences for estimating power consumption of sequential circuits for which there exists an initial automaton description. The process of forming such a test sequence can be viewed as traversing a walks through the line digraph of the circuit automaton model. Different types of traversals which could meet different requirements were proposed.

LITERATURE